Elevating 3D NAND performance: Dogwood and Its Process-Property Correlation for Low Resistivity, High Speed, and Superior Cell Performance

Dr. Lakshmi Suresh [1]*, Micron Technology, Singapore**; Swapnil Lengade[1],** Micron Technology, Boise, Idaho, United States of America**; Roland Mok[1],** Micron Technology, Singapore**; Dr. Haoyu Li[1],** Micron Technology, Boise, Idaho, United States of America**; Ramanathan Gandhi[1],** Micron Technology, Singapore**; Rita Klein[1],** Micron Technology, Boise, Idaho, United States of America, **Chieh Hsien Quek[1],** Micron Technology, Singapore.

***Corresponding author:**

Dr. Lakshmi Suresh,

#03-11, block 12, Adana @ Thomson,

Singapore 573870

Email: lsuresh@micron.com, Ph: +6587005887

[1] Technology Development, Micron Technology

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Abstract: A significant breakthrough in fluorine-free Dogwood (DW is a Micron Codename for a first-of-a-kind WL metal) wordline processing for 3D NAND flash memory has been realized. The integration of DW into WLs enhances both vertical and horizontal cell scaling, yielding substantial reductions in resistance-capacitance (RC) delay and lower leakage failure rates compared to tungsten (W) counterparts. Key to this development is process optimizations aimed at minimizing oxygen impurity, a critical factor in improving resistivity and work function stability. By optimizing deposition parameters such as partial pressure, precursor concentration, and purge cycles, oxygen residues within DW films can be effectively mitigated. Optimizing hydrogen partial pressure, reaction chemistry through precursor tuning during deposition enhances reduction reactions, improving film purity. Novel chemical surface treatments and optimized ALD cycling techniques eliminate oxygen contamination in DW voids, driving down resistivity and boosting speed performance. This fluorine-free process directly addresses key issues like read disturb and charge loss, closely tied to metal fill and work function degradation. Through fine-tuning DW film growth dynamics and reducing oxygen incorporation, the process achieves superior electrical properties with larger grain structures and higher uniformity. Collectively, these advancements extend the scaling limits of 3D NAND memory, offering a pathway to achieve low resistivity and high-speed operation with exceptional cell performance. This DW-based process is a vital innovation for next-generation 3D NAND flash technologies, supporting the increasing demand for high-density, high-performance memory.

Keywords: **Thin Film deposition, Dogwood, Read-Disturb charge loss, Work function, grain size, Metal WL fill, tier deflection, impurity reduction.**

I. INTRODUCTION

With significant advancements in automotive and mobile industry, the booming era of cloud data traffic, and the industry's never-ending appetite for solid-state drives (SSDs), it is imperative for the storage industry to work towards high performance and vast storage devices. With such continuous needs and eminent competition with respect to both technology and market share, it was crucial to intercept the most advanced NAND with Dogwood (DW) metal as wordline for its non-fluorine-based precursor which help eliminating tier oxide damage. For the first time in 3D-NAND history, this new metal has been explored for its material, electrical and chemical behavior. DW/Alternative metal is increasingly critical in the development of 3D NAND devices due to its unique properties and compatibility with advanced semiconductor manufacturing. As device geometries shrink and layers in 3D NAND stacks increase, traditional materials struggle to meet the stringent requirements for conductivity, durability, and manufacturability. From a scaling stand point, the DW's low resistivity and non-fluorine chemistry make it an ideal candidate for use as a metal barrier, electrode, and interconnect material in these densely packed devices. Its ability to maintain integrity at elevated temperatures ensures reliable performance in complex, multi-layered architectures, while its lower diffusion rate reduces contamination risks. Additionally, DW's work function tunability makes it suitable for advanced gate stacks, which are key for the next generation of NAND technologies[1]. As 3D NAND devices push the limits of memory density and performance, DW offers the necessary scalability, improved yield, and enhanced electrical performance, making it a vital material for the future of data storage technologies.

II. BACKGROUND & CHALLENGES

The importance of minimizing RC (resistance-capacitive) delay and mitigating tier oxide damage in NAND metallization is a critical area of research in semiconductor device engineering, particularly as memory devices move toward advanced nodes and 3D architectures. RC delay, caused by the resistance of interconnects and the capacitance between adjacent lines, directly affects the switching speed and overall performance of NAND flash memory. As device dimensions shrink and the number of vertical layers in 3D NAND increases, the length and complexity of interconnects become greater, compounding the RC delay problem. Tungsten (W) has traditionally been used for wordline (WL) and bitline (BL) interconnects due to its robustness and well-understood deposition methods, such as chemical vapor deposition (CVD) and physical vapor deposition (PVD). However, tungsten's relatively high resistivity (~5.6 μΩ·cm) makes it a limiting factor for further scaling, prompting the exploration of alternative metals like molybdenum (Mo), cobalt (Co), and ruthenium (Ru) that promise lower resistivity scaling and better performance in advanced nodes (Fig 1).

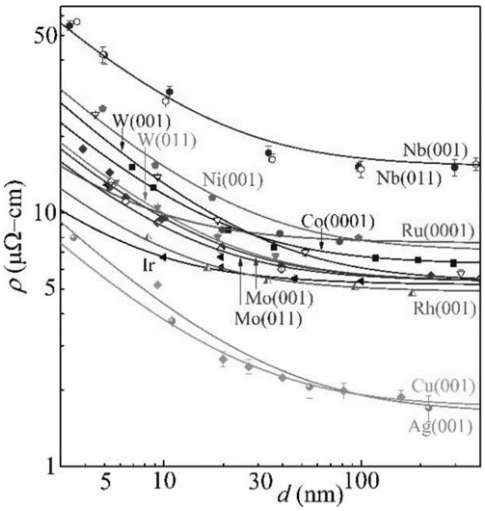
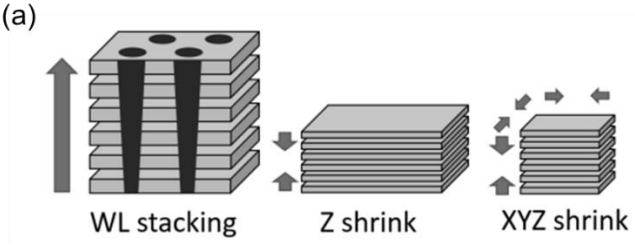


Fig 1: Effective resistivity vs feature thickness d for different metals in epitaxial layers

Another key issue in the metallization of advanced 3D NAND structures, is the formation of voids within the deposited layers, particularly as the aspect ratios of wordlines increase with additional tiers. These voids can cause significant reliability issues, such as increased resistance, electromigration failures, and, ultimately lately, device breakdown. The challenge is to develop metallization processes that can fill these high-aspect-ratio structures without creating voids while maintaining low RC delay. The hypothesis driving much of the recent research is that by using alternative metals with lower resistivity and employing advanced deposition techniques like atomic layer deposition (ALD). Doing so, it is possible to reduce both RC delay and void formation, thereby improving device performance and reliability.

(a)



(b)

	$\lambda\times\rho$ (10^{-16} Ω-m^2)	λ (nm)		$\lambda\times\rho$ (10^{-16} Ω-m^2)	λ (nm)
Rh	3.2	6.9	In	7.6/7.2	8.7/8.2
Pt	3.43	3.23	W	8.2	15.5
Ir	3.7	7.1	Au	8.3	37.7
Nb	3.91	2.57	Ag	8.5	53.3
Ni	4.1	5.9	Mg	9.8/8.8	22.3/20.0
Al	5	18.9	Zn	10.3/8.1	17.4/13.7
Ru	5.1/3.8	6.6/4.9	Ca	11.9	35.4
Mo	6	11.2	Cd	12.6/11.3	16.8/15.1
Os	6.4/4.3	7.2/4.9	Na	14.7	30.9
Cu	6.7	39.9	Be	17.1/24.3	48.0/68.2
Co	7.3/4.8	11.8/7.8	K	22.7	31.5

Fig 2: (a) XYZ scaling scope in 3D NAND, with stacking along Z and footprint reduction in XY direction and (b) Product of the bulk resistivity times the bulk mean free path λ_Q from first-principle predictions

Several scientific studies have examined the potential of alternative metals to replace tungsten in advanced semiconductor interconnects. Molybdenum (Mo), for instance, has garnered attention due to its lower resistivity (~5 μΩ·cm) compared to tungsten. Studies by Kim et al. (2020) and Yu et al. (2019) have demonstrated that ALD Mo can offer conformal deposition in high-aspect-ratio structures, reducing the likelihood of void formation. Moreover, the resistivity of Mo can be further lowered through doping or annealing processes, as outlined in research by Yamamoto et al. (2021). Ruthenium (Ru) is another promising candidate due to its relatively low resistivity (~7.6 μΩ·cm) and excellent electrochemical properties, making it a good option for reducing electromigration concerns. Studies such as those by Takahashi et al. (2021) have shown that Ru can be deposited using CVD or ALD, providing a void-free fill in 3D structures (Fig 2b).

Modeling efforts to address void formation in these metal deposition processes are critical. Researchers have developed simulation tools to predict void formation based on deposition parameters, such as precursor flow, temperature, and pressure, and to understand the impact of metallization on RC delay. Studies by Jung et al. (2021) and Wang et al. (2020) have shown that voids tend to form in areas with poor step coverage and inadequate precursor diffusion. Their models suggest that fine-tuning the deposition process, combined with the inherent material properties of metals, can lead to improved fill quality and reduced void formation.

The scaling trajectory of 3D NAND technology relies on two primary strategies: vertical scaling, which entails increasing the number of layers while reducing tier pitch, and lateral scaling, where XY dimensions are shrunk (Fig 2 a). Both approaches critically influence wordline (WL) resistance and overall device performance. These scaling methods, while enhancing storage density, introduce significant challenges, particularly in terms of managing WL resistance and achieving effective metal fill [2].

1. Vertical Scaling: Tier Pitch Reduction and Increased Layer Count

A key advancement in 3D NAND is vertical scaling, where manufacturers progressively increase the number of stacked memory layers to boost storage capacity without enlarging the chip's XY area. This increase is often coupled with a reduction in tier pitch—the vertical distance between layers—to limit the overall stack height. However, decreasing tier pitch often reduces the cross-sectional area of the wordlines. As a result, the resistance of these conductive paths rises, potentially slowing down read and write operations and affecting signal integrity. The greater resistance, caused by smaller wire geometries, necessitates the development of new metallization processes or materials that offer lower resistivity while maintaining the mechanical and electrical integrity of the 3D stack.

2. Lateral Scaling: Shrinking the XY Dimensions

Alongside vertical advancements, lateral (XY) scaling reduces the physical footprint of individual memory cells, increasing the number of cells within a given chip area. This approach helps meet the growing demand for higher memory densities. However, shrinking the lateral dimensions lengthens the wordlines, exacerbating resistance-related issues. As the cell width decreases along with block width increase, wordlines must cover greater distances, and their reduced cross-sectional areas further elevate resistivity. The increased WL resistance can degrade device performance by slowing access times and increasing power consumption. Consequently, controlling WL resistance in lateral scaling becomes critical, necessitating advances in conductor materials and deposition techniques to maintain performance as dimensions shrink.

3. Impact on Metal Fill and Block Pitch

The block pitch—the horizontal spacing between groups of memory cells—plays a crucial role in determining the packing density of 3D NAND devices (Fig 3). A larger block pitch can enable denser memory arrays, but it also impacts the metal fill process during manufacturing. Metal

fill becomes increasingly challenging in high-density structures due to the narrow spaces between wordlines and bitlines.

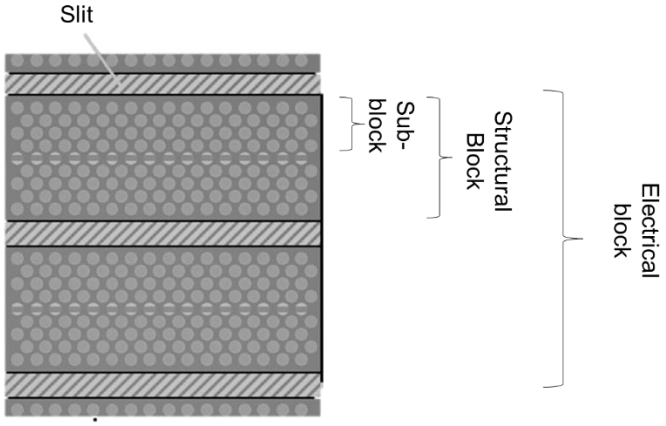


Fig 3: An example of block architecture in 3D NAND

Incomplete or uneven fill can lead to voids, which in turn increase the effective resistance of the interconnects and reduce device reliability. Tier oxide damage during tungsten deposition often result from fluorine attack, where etching gases like tungsten hexafluoride (WF6) and HF release fluorine atoms. These fluorine atoms can diffuse into the deposited layers or sidewalls, leading to microstructural weaknesses[3] (Fig 4). Over time, the aggressive nature of fluorine creates voids at the grain boundaries or between tiers, especially at high temperatures. These voids can cause critical defects such as delamination, poor step coverage, or electrical failure in multilayer semiconductor stacks. Careful control of fluorine by-product concentration, temperature, and deposition conditions is essential to minimize these voids and ensure high-quality, reliable tungsten fill. Achieving high-quality, uniform metal fill in these scaled structures requires precise control over deposition techniques like atomic layer deposition (ALD) and chemical vapor deposition (CVD), as well as optimization of process parameters to minimize void formation and ensure low-resistance, defect-free interconnects.

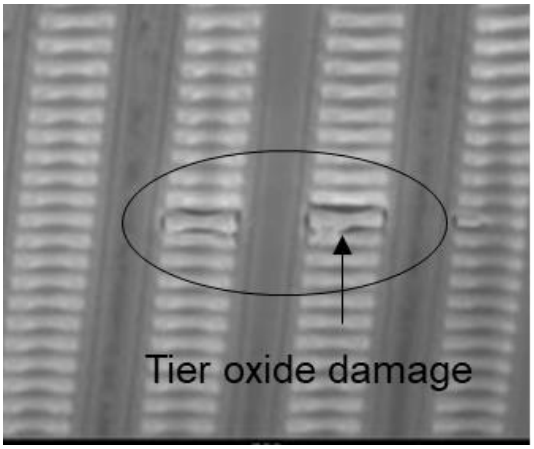


Fig 4: Tier void formation in Tungsten based 3D NAND structures due to byproduct attack on the oxide interfaces

In conclusion, reducing RC delay and eliminating tier voids are crucial for scaling 3D NAND technology. Tungsten's limitations in resistivity have spurred interest in alternative metals like molybdenum, copper, cobalt and ruthenium. These materials, along with advanced deposition techniques like ALD and optimized process parameters, offer promising solutions to the challenges posed by RC delay and void formation. Ongoing research in this area, particularly focused on optimizing deposition processes and material integration, will be pivotal in driving the next generation of NAND devices. And as, 3D NAND scaling progresses through increased vertical layer stacking, reduced tier pitch, and lateral shrinkage, maintaining low wordline resistance and achieving effective metal fill become critical technical challenges. Addressing these issues through material innovations and advanced deposition technologies is essential to sustain performance and reliability in future generations of 3D NAND devices.

III. Methodology & Mechanisms

A. DW Deposition

This work focuses on using the ALD deposition technique to deposit DW films. The current technology can deposit DW through a series of Liner and Bulk film reactions between a non-fluoride based DW precursor, Ammonia and Hydrogen. The hardware used in this study has a 4-pedestal system constituting 4 stations, with dual zone heating system, individual charge volumes for all stations for the precursors, reduction and purging gases. Precursor concentrations between 1.0 % to 8%, ammonia concentrations between 25-100% and bulk temperatures between 500-614^{0}C. Despite the pressure or process regime,

the DW deposition starts with a thin in situ liner deposition in pedestal 1 and is followed by liner conversion and bulk deposition in pedestal 2, 3 and 4. (Fig 5)

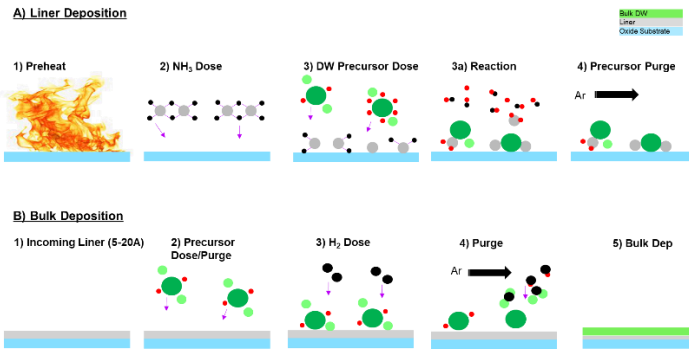


Fig 5: DW ALD deposition flow adapted for better WL fill in advanced NAND structures

ALD of DW presents significant challenges when performed on dielectric surfaces, particularly when a Insitu-liner is not employed. A key challenge is the nucleation delay, driven by the interaction of the precursor with the dielectric surface. The nucleation delay is primarily attributed to the lack of sufficient bonding sites on the oxide surface, which inhibits the adsorption of precursors. Specifically, surface defects and hydroxyl (OH) groups play a critical role in this interaction, where the bonding and thermal reduction steps result in the formation of undesirable DW oxides and oxychlorides[4].
In a simplified form, the ALD reaction is:

$$DWX_{\alpha}Y_{\beta} + ZH_2 \rightarrow DW + HX + HY \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Here, while DW is deposited, we have H_2X and HY released as by-products. The reaction is facilitated by elevated temperatures and pressures, which promote DW nucleation on the surface. However, the distorted precursor and transitional reaction structures tend to have a sluggish and complicated nucleation[6]. Nucleation on dielectric surfaces is typically sluggish due to the limited availability of reactive sites. As a result, higher temperatures (>600°C) are required to achieve reasonable nucleation rates without a liner. Without a liner, DW ALD requires temperatures above 600°C to reduce nucleation delay. At 550°C, the delay exceeds 200×, reducing to 80× of DW deposition ALD cycles at 600°C (Fig 6). While higher temperatures accelerate nucleation, they also increase the risk of substrate damage due to interactions with precursor chemistry, potentially causing chemical degradation of the dielectric. Without a liner, the slow nucleation leads to discontinuous film morphology, especially on dielectric surfaces. This leads to poor step coverage and high surface roughness, which can degrade the performance of the final device. Additionally, the high process temperatures required to mitigate nucleation delay introduce integration challenges due to the limited thermal budget of semiconductor processes. The evolution of by-products such as H_2X and HY during the bulk deposition process also plays a significant role in the process efficiency. The efficient removal of these by-products via high gas flows of process gases is essential for maintaining surface cleanliness and avoiding unwanted side reactions. Precursor concentration tuning is critical for improving wordline fill in high aspect ratio structures. By optimizing the precursor dose and carrier gas flow, the deposition process ensures uniform coverage throughout the trenches. Proper tuning minimizes void formation, enhances step coverage, and reduces the risk of nucleation delays or film defects. Additionally, adjusting the reduction gas flow balances precursor saturation, improving film uniformity and electrical performance.

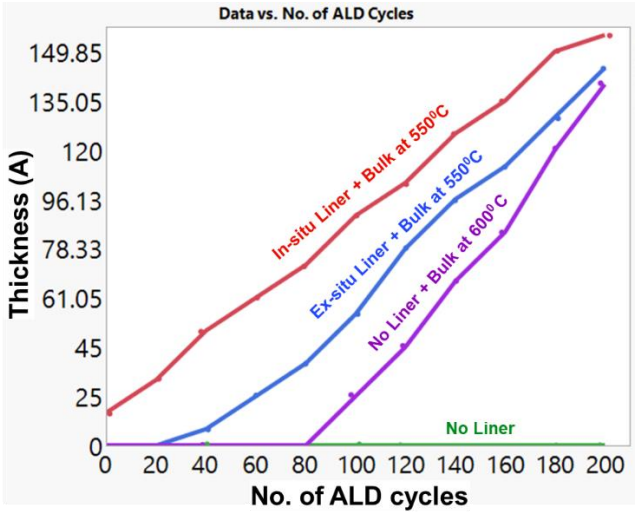


Fig 6: DW growth rate on different substrates, some showing higher nucleation delay than others

B. Thermodynamic principles driven material property optimization.

A study on ruthenium (Ru) thin films grown via atomic layer deposition (ALD) using specific precursors and oxygen was recently published in Journal of Material Science C. Intrigued by that research, and hypothesis of oxygen playing a critical role in determining the grain size and surface morphology of the films was conceptualized. Higher oxygen doses lead to increase in oxidation, which could impact the film's crystalline structure and surface smoothness. By controlling the oxygen exposure, it is possible to achieve smoother surfaces and desirable grain structures, highlighting the importance of precise oxygen management in ALD processes[7].
The hypothesis regarding the impact of oxygen and temperature on grain size suggests that oxygen can hinder grain boundary migration. This results in smaller grains, as the boundaries are less mobile in the presence of oxygen. On the other hand, higher deposition temperatures tend to

lower the oxygen content. This reduction in oxygen allows the grain boundaries to migrate more easily, leading to the growth of larger grains.

This dual influence of oxygen and temperature is critical for optimizing the ALD process. By controlling these factors, it becomes possible to achieve low resistivity and the desired grain structures in metal thin films. The underlying thermodynamic principle of this hypothesis is that grain growth is driven by a reduction in the system's overall free energy. This reduction in energy is accomplished by decreasing the total grain boundary area.

Oxygen adsorption at grain boundaries increases the boundary energy, thereby inhibiting grain boundary migration and stabilizing smaller grains. According to nucleation theory, higher oxygen levels promote the formation of numerous nucleation sites, leading to finer grain structures. Conversely, higher temperatures facilitate atomic mobility, enhancing grain boundary migration and growth. This aligns with classical growth theories, where increased temperature reduces the activation energy for atomic movement, promoting larger grain formation.

C. Structural Validation

The increase in grain size is significant as it directly correlates with improved electrical conductivity and reduced grain boundary scattering. Additionally, the grain orientation distribution in optimized DW films is more uniform, with a higher fraction of low-angle grain boundaries, indicating a higher degree of crystallographic order and fewer defects. This enhanced grain structure results from the optimized deposition conditions that favor grain boundary migration and growth, facilitated by the controlled introduction of oxygen and precise temperature regulation during the ALD process. Transmission electron microscopy (TEM) methodology was utilized to measure the grain size on structure wafers for 3 kinds of DOE wafers. For pressure tuning (P) and pressure + concentration tuning (PC), the grain sizes were found to be relatively smaller and less uniform compared to those achieved with pressure + concentration tuning + interfacial conversion temperature tuning (PCT). Specifically, the grains in the later films were larger, particularly around the interface, indicating enhanced grain growth and stability. Additionally, wordline fill analysis using TEM provided further insights into the quality of the fill process. (Fig 7 a)

TEM imaging revealed that the PCT process resulted in 4% better fill with fewer voids within the wordlines, demonstrating superior fill uniformity and density (Fig 7 b). This improvement is due to the optimized deposition parameters and refined precursor chemistry, which promote better adhesion and layer formation during the deposition process. Consequently, this film exhibits improved electrical and mechanical properties, making them more suitable for advanced semiconductor applications where high-quality fill and grain structure are critical.

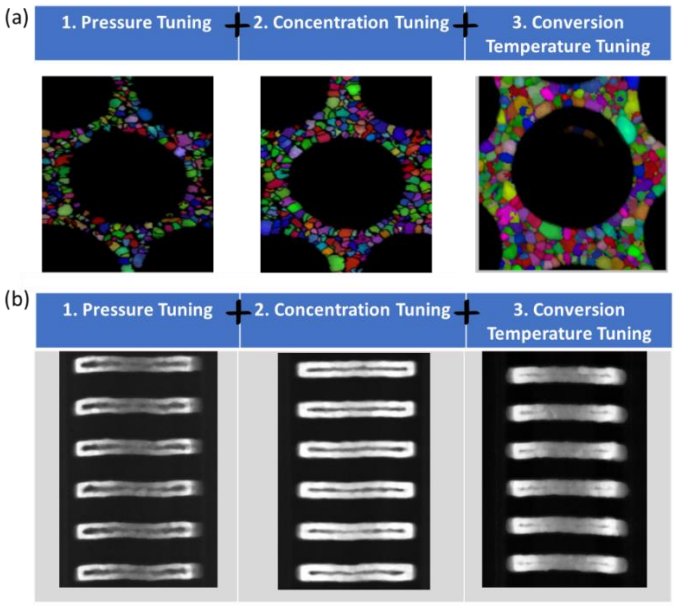


Fig 7: Impact of process optimization on the (a) Grain size of DW and (b) wordline fill

IV. Electrical Behaviors

In NAND flash memory, the wordline (WL) metal properties significantly impact key device parameters such as, Retention, Read disturb, Program disturb, Threshold Voltage, Latency etc. The metal used for wordlines must have high thermal and oxidation stability to maintain the integrity of the WL over time. Poor metal stability can lead to electromigration, affecting the charge stored in memory cells and thus degrading retention. WL metals must exhibit low resistivity to minimize voltage drops during read operations. Higher resistivity can increase RC delay, leading to higher read disturb, where unintended charge shifts occur in neighboring cells. Robust metals with strong electromigration resistance ensure consistent wordline performance under high electric fields during programming. Instabilities or voids in the WL metal could cause uneven voltage distribution, increasing program disturb (Fig 8). The stability of the WL metal impacts how consistently the desired voltage is applied across memory cells. WL metal degradation over time can cause Vt drift, making it harder to distinguish between programmed states. With the DW development and optimizations, these critical device metrics were improved especially wordline resistance, threshold voltage and read disturb enabling the most advanced NAND product for Micron.

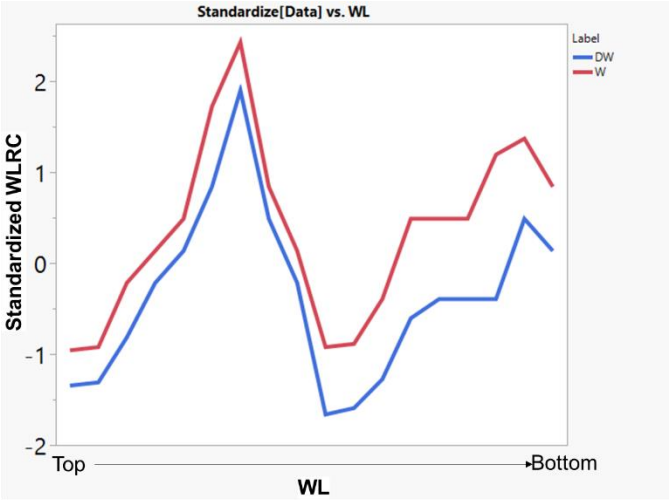


Fig 8: Demonstration of improved WL RC delay with the new metal DW over traditional W

V. Conclusion

This study of DW deposition processes, including P, C, PCT kinds, highlights significant advancements in the performance and reliability of 3D NAND structures. TEM analyses reveal that PCT consistently produces larger grain sizes and achieves superior wordline fill quality compared to its predecessors. The key challenges faced in the integration of this new metal was done through innovative solutions in a multi-disciplinary approach. This includes various process optimizations, integration changes such as Dry Etch and Wet Process to establish-reestablish the material property interactions and influence on electrical properties.

VI. Acknowledgements

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