ATE Multi-Site Hardware Design for Wi-Fi 6E and BT Devices

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Abstract - This article is to summarize best practices and guidelines for designing multi-site automatic test equipment (ATE) PCBs for testing of Wi-Fi and BT combo products. As the frequency, bandwidth and performance requirements becomes higher, the design of ATE test load board becomes more crucial. The parasitic capacitance of PCB itself and Electro-Magnetic Interference (EMI) between traces can significantly degrade RF performance. The preference is to design for multi-site parallel testing to improve test efficiency and reduce cost nowadays, thus signal integrity and isolation are important factors in the PCB design. Moreover, we need to take DC power plane, layer to layer, digital signal isolation and proper grounding into consideration as well.

In the Introduction section, we will briefly describe the feature of our device under test (DUT) and the background of our automatic test equipment (ATE). Most of the devices we test are Wi-Fi and BT combo chips, for example SYN43756E is a tri-band (2.4G, 5G, and 6G) Wi-Fi 2×2 MAC/Baseband/Radio with integrated Bluetooth (BT) 5.3. The automatic test equipment (ATE) platform we use is Teradyne UltraFlex; this tester platform provides excellent signal quality, sufficient site count and flexible configuration with existing applications.

Next in Methods section, we will start from load board schematic design, including component selection which are mostly RF switches, noise coupling capacitors, and ferrite beads, then components placement, and finally routing evaluations. Taking our board as an example, first thing to consider for component selection and placement is space constraints due to multi-site design. Trace routing and layout of critical signals like RF takes precedence in the design. The RF traces are routed on the top layer with ground layer right beneath it; the space between RF traces is suggested greater than 780 mil [1], however, for multi-site RF ATE solution PCB, the space is constrained and limited, so we use ground stitching or ground shielding for RF signal isolation. [2] In addition, we also performed simulation based on RF traces dimension and physical layer's definition for S-parameters estimation. It is trade-off between signal integrity and multi-site efficiency, so we must be considered thoroughly before PCB fabrication. We will demonstrate our test result based on the board we have for SYN43756E, we can get around -35dB error vector magnitude (evm) level in 7115MHz BW20MHz at 10dBm transmit power level with channel estimation off; constellation plots by using Keysight 89600 VSA 20.4 will be shown later in this article. From test cost and efficiency perspective, we have 8 sites ATE test solution which show high multi-site efficiency and low cost.

Based on our experience and achievements, we would like to deliver a successful, concise, easy to implant PCB design considerations and guidelines for reader to apply on multi-site Wi-Fi 6E or cutting-edge Wi-Fi products automated test equipment (ATE) device interface board (DIB) design.

Keywords: ATE, RF, Load board, Design, Multi-site

1. Introduction

This article demonstrates PCB design guidelines based on our experience of designing ATE load boards for testing Synaptics Wi-Fi and Bluetooth combo chips. Taking Synaptics SYN43756E as an example, it is a Tri-band (2.4GHz, 5GHz and 6GHz) Wi-Fi 2×2 MAC/Baseband/Radio with integrated Bluetooth (BT) 5.3. 20/40/80 MHz channels for 5/6Ghz radio, and 20/40 MHz channels for 2.4Ghz radio with 1024-QAM modulation support on both 2.4Ghz and 5/6Ghz. On-chip power amplifiers and LNAs for both bands and support for external LNAs. Client MU-MIMO. Supporting worldwide homologated design, including IEEE 802.11d/h. [3]

Synaptics SYN43756E single-chip device includes an integrated 2.4/5/6 GHz IEEE 802.11 a/b/g/n/ac/ax MAC/baseband/radio, real simultaneous dual band product. It also supports Bluetooth 5.3 and Bluetooth Low Energy (BLE). Figure.1 is the interconnect of all

the major physical blocks in the SYN43756E and their associated external interfaces.

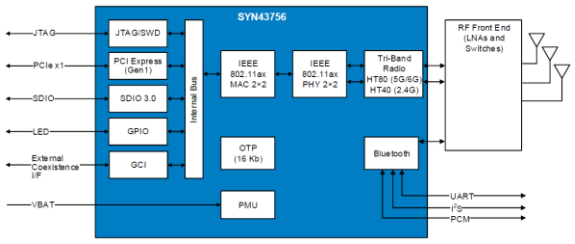

Figure.1 SYN43756E Functional Diagram

The automatic test equipment (ATE) we use is Teradyne UltraFlex with MX8 instrument that extends frequency range up to 7.5GHz to support Wi-Fi 6E testing. This RF instrument supports 1024QAM for WLAN with 16 fully calibrated bi-directional ports, while only 8 of the ports can source and capture signals in parallel. Low Phase Noise Microwave Source using integrated High Performance LO Synthesizers provides < -40 dB error vector magnitude (EVM) for 80MHz 802.11ax and < 0.8dB absolute accuracy with calibrated power detectors. With VSA toolkits, we could use library of modulated waveforms and software algorithms optimized for throughput along with background DSP.

2. Methods

We utilize conducting transmit instead of antenna for RF signal traveling in our ATE load board. With standard ATE load board design process, we will start from site and channel arrangement, schematic and component selection, placement of critical components for multi-sites, routing, layer arrangement, and simulation for critical nets.

2.1 Schematic and Components Placement

We have enough digital channels from HSD, power supplies from both DCVS and DCVI from Teradyne UltraFlex. The critical limitation for us to determine maximum site count is RF instrument. As there are 8 independent ports in MX8, we define 8x solution for SYN43756E, a dual 6G core and BT combo device. Both cores share the same RF instrument and users could perform the selection by using RF switches.

For RF testing path, we try to make path between chip transceiver end to SMP port as short and simple as possible to reduce impedance mismatch thus we only have DC coupling capacitor, a power attenuator to protect tester instrument and RF switch in this path.

To achieve best of the performance, test engineer should select a proper switch for RF purpose. The switch we use is PE42540, a four-port RF switch with high resolution particularly support for test equipment and ATE market. It can be used from 10 Hz to 8 GHz, applicable for high frequency and low insertion loss. [4]

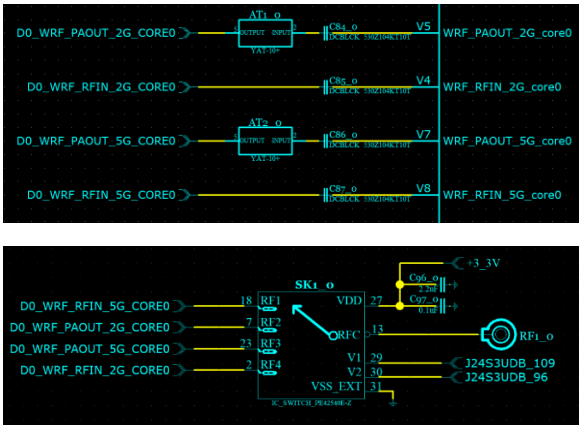

Figure. 2 RF circuit from DUT to SMP port

For SYN43756E XTAL clock input, we use UltraFlex internal instrument DUT CLK as clock resource, and to a monolithic crystal filter to get a precise clock for chip radio usage. The DUT CLK instrument supports up to 100Mhz and with programmable power level. XTAL clock to the chip needs to be very clean and accurate for RF testing, so components along the XTAL clock path should also be placed as close as possible to the chip and the traces should be properly isolated. However, because size of crystal filter is big(Y1), it cannot be put very close to DUT, the filters are about 10 centimeters away from DUT. By measuring clock waveform by oscilloscope and test result, it is acceptable to place crystal filter slightly away to make room for DC coupling capacitors, attenuators and RF switches close to DUT.

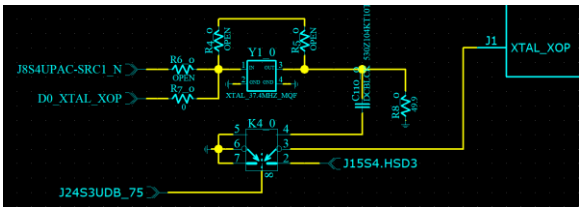

Figure. 3 Xtal pin circuit design

Power supply for RF products could affect RF performance significantly, thus decoupling caps are put close to DUT as convention. The capacitors size

we choose to decoupling noise of power supplies is 0201.

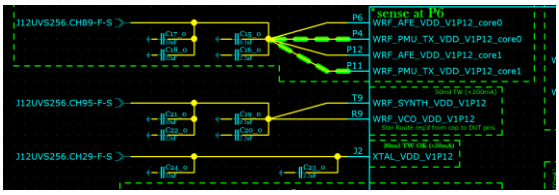

Figure. 4 Power pin circuit design

We would like to place most of the components as close to the DUT as possible; however due to component size and multi-site load board space constrains, we have around 2- 3centimeter diameter for octal site. Thus, we can only put most critical and smaller enough components, like decoupling capacitors close to DUT. Decoupling capacitors can filter out noise from the DUT to prevent it from reaching out to DUT. Power supply noise in the radio can increase phase noise of the frequency synthesizer, resulting in poor signal quality [4]. Aligning similar components in the same direction could help effective routing and make less soldering mistake as well.[7]

2.2 Routing

Routing is the process of connecting components on PCB, or ATE load board. The longer the trace, the greater of its resistance, capacitance and inductance and there will be more possibilities for traces' cross talk. In addition, we should keep trace width consistent to make sure impedance is even. If traces need to take turns, we could take turns with angles of > 90 degrees and avoid sharp angles or 90 degrees bending to prevent signal reflection.

PCB parasitic is a natural characteristic of the PCB itself that has an impact of circuit performance. It is a virtual capacitor formed between two conductive layers with insulated material in between. We can evaluate parasitic by using calculators by inputting dimensions to online calculators for capacitive and inductive effects. Normally we are seeing inductance level in the order of nH, and capacitance is on the level of pF. When we are going to test RF or high-speed products, the parasitic could potentially damage test performance; for example, the capacitance may behave as band pass filter in transmission lines, or causes noise coupling between grounds with different signals, which results in common mode noise. To mitigate parasitic effects, we could use ground shielding for sensitive traces, increase space between traces, and reducing parallel traces design. When parallel wiring is used, the area between metals is the largest and the parasitic capacitance is also the highest.[6] Last but not least, overuse of vias can also increase parasitic inductance and capacitance. Vias are used to connect different layers, when users dealing with RF, high speed, high data rate signals, need to consider via parasitic capacitance and inductance which may leads to crosstalk and cause signal distortion.

Signal layer should be sandwiched by two ground layers or between a ground layer and a power layer. In our design, RF signals are not only on top layer or sandwiched by ground layers, but also arrange same frequency RF traces in the same layer, not fully parallel, and ground stitching while ground shielding for EVB to isolate critical traces to achieve better performance for coexistence of RF signals.

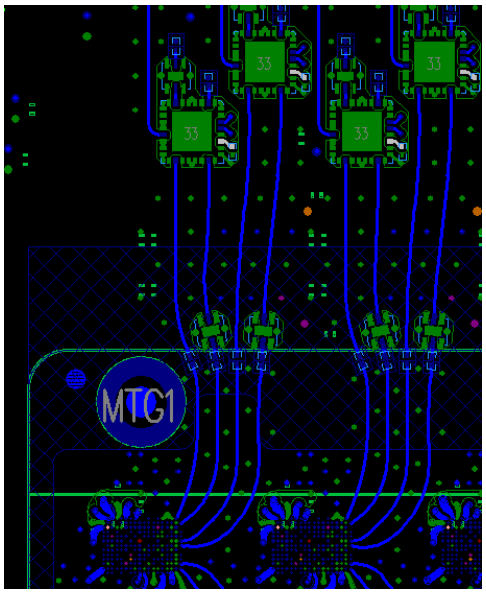

Figure. 5 6G signal routing on top layer. Traces are not fully parallel, with ground stitching.

2.3 Stack-Up

SYN43756E ATE load board is a complex design composed by 46 layers; the main reason of that many layers is because we insert ground layers in around each signal layer to reduce signal interference. Ground layer are very important in RF PCB design. The return path of RF signal is to the ground layer right beneath RF traces, so ground layer should be as wide as possible to prevent any discrepancy which cause small current loop on the particular path, thus affecting overall impedance matching [5] There are 3 of RF ports, two Wi-Fi and one BT for SYN43756E, and we have limited space for each DUT in multiple site load

board, so RF traces are located in 2 layers, 6G RF traces are on top layer, and 2.4GHz lines are on the 3rd layer with ground layer in between.

2.4 Simulation

By inputting actual dimension of the RF traces to PCB impedance calculator, top layer RF trace impedance is estimated 50.1Ω. For 2.4GHz lines located in layer 3 sandwiched between ground layer 2 and layer 4, we could match the impedance to about 50.1Ω, even with the 10mil spacing, we are almost at the same number (49.5Ω)

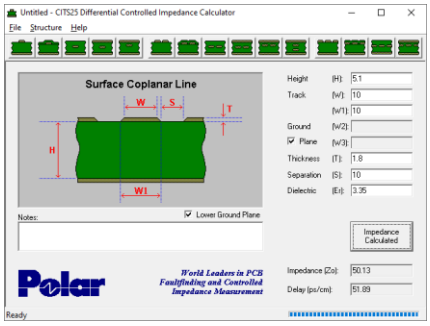

Figure. 6(a) Top layer trace impedance calculator

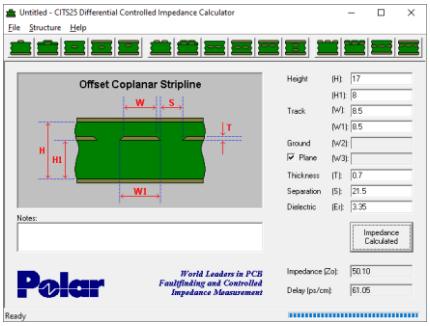

Figure. 6(b) Layer 3 trace impedance calculator

2.5 S parameters

In addition to impedance, we also perform S_{11} and S_{21} simulation for signal quality and power loss evaluation. S_{11} is the input reflection coefficient with the output of the network with matching load. S_{21} is the forward transmission loss. Generally, $S_{11} \leq -10$ dB is considered sufficient. Table. 1 illustrate the return loss (dB) of incident signal, and power reflected (in dB), and percentage of transmission [5].

S_{11} (dB)	Return Loss (dB)	Reflection Loss (dB)	$P_{transmit}/P_{incident}$ (%)
-20	20	0.04	99
-10	10	0.46	90
-3	3	3	50
-1	1	7	21

Table. 1 Return Loss, Reflection Loss and Forward Power %

10dB return loss means that the 90% of the incident power goes into output for transmission while 10% of power reflects to incident side. Taking 6G trace from RF switch (SP4T) to SMP connector (RF1) as example, S_{11} is around -32dB which means the impedance of 6G transmission line is very close to 50Ω, and S_{21} is around -0.22dB represents loss is around 0.22dB, also represents the trace is with good matching. For critical traces like 6G, 5G, 2.4G and BT, users could determine whether need to perform simulation to ensure the impedance is as expected before fabricating the actual board.

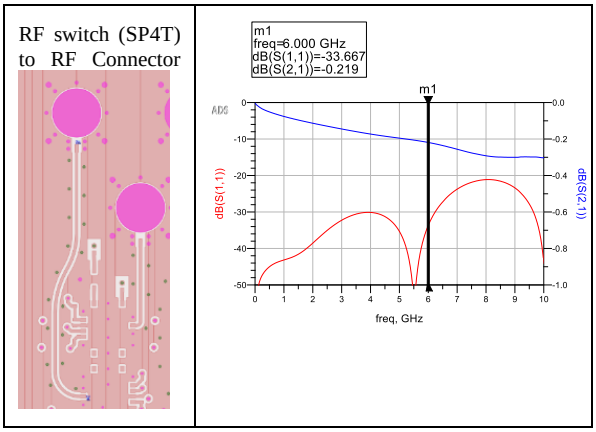

Figure. 7 S-parameter simulation for 6G trace, from RF connector to RF switch

3. Results

By selecting proper components which are specially design for RF usage, applying proper dimension, spacing between sites, grounding and shielding, simulate before fabrication, we should have more assurance and confidence to manufacture ATE load board. PCB design criteria may vary depends on different products characteristics and application requirements. We would like to make a general guideline so test development engineers can make ATE hardware more effective, save unnecessary cost and time to build a robust ATE load board for RF products. Theoretically we would like to have impedance equals to 50Ω at target test frequency, we could calculate insertion loss by reviewing S-parameters. To test multi-site in parallel, we use ground shielding for RF traces, use cables for long distance transmission, ground layers isolation between RF, analog and digital layers to prevent crosstalk and to reduce parasitic capacitance.

Figure. 8 below is the error vector magnitude (EVM) plot by VSA tool Keysight 89600, capturing Tx signal

from chip during multi-site testing. We can determine whether there is IQ gain or phase mismatch from constellation plot. Based on digital signal processing (DSP) calculation result, we can get EVM around -32 to -35dB while transmitting 10dBm signal at 7115MHz, BW=20MHz OFDM, 256- QAM (R = 3/4), cyclic delay diversity (CDD). Comparing with bench result, we may have 2 to 3 dB EVM lower due to wafer probing instead of direct soldering on bench, but ATE result is very close to datasheet typical value which is -32dB at 12.5dBm at the same frequency and data rate.

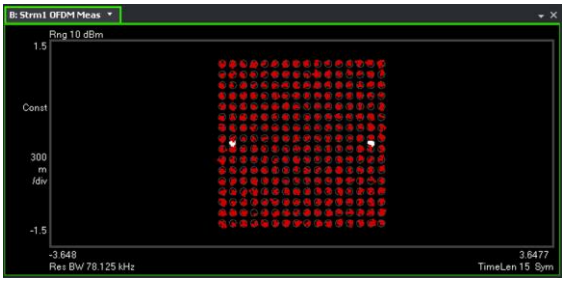

Figure. 8 256-QAM constellation plot at 7115MHz BW20MHz with 10dBm transmit power

Taking SYN43756E 8x sites ATE solution as example, we can achieve parallel test efficiency around 92%, and wafer level test cost is less than 2.5% which is significantly low. This result also inspires us RF testing with high end ATE could also be cost effective.

4. Summary and Future work

In this article, we emphasized on the importance of selecting RF compatible components, trace design, spacing, grounding and simulation that should be considered, and things need to be prevented to reduce parasitic capacitance before fabricating a RF ATE board. The guidelines in this article are based on the studies and experiments we have for Synaptics RF products ATE load boards. By using these methods, we should be able to reduce hardware and test cost. Making ATE load board on time delivery which leads to new products engineering sample on time delivery and mass production on schedule.

To optimize ATE fabrication preparation, in the future, we may also consider matching network for RF circuit to provide a better performance. Also, we could use network analyzer to validate trace impedance and compare it with simulation result. In addition to load board PCB simulation, we could consult design team for simulation collaboration, there is transmission line model in design simulation library for coplanar line. As long as we can provide trace impedance and length, designers are able to evaluate load and delay from chip. Wafer level testing needle type is not mentioned in this article but is also crucial for RF testing. We would like to include a more comprehensive guideline for ATE test development engineers to reduce design period in a high performance and cost-effective way.

Reference

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