Highly Efficient Auto Batch EFA

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Abstract - This study presents a novel testing methodology for highly efficient auto batch Electrical Failure Analysis (EFA), capable of identifying all failures within a few hours. This approach enables the automatic generation of standardized failure analysis reports, achieving a speed that is 100 times faster than traditional manual processes. The primary advantage of this innovation lies in its ability to conduct comprehensive testing and analysis of failed samples, thereby offering critical insights that enhance the feedback loop to the fabrication process and improve factory test coverage. This advancement not only streamlines the failure analysis workflow but also significantly contributes to overall production efficiency and quality assurance.

I. Introduction:

In the semiconductor industry, the Early Failure Rate (EFR) test is a critical qualification process for assessing the Defect Parts Per Million (DPPM) levels of devices. Typically conducted on a scale of 10,000 to 100,000 dice, the EFR test often results in the identification of numerous defective devices that require Electrical Failure Analysis (EFA) to determine the underlying failure modes.

Traditionally, EFA has been performed manually, with each defective device analyzed individually through bench testing. This approach poses significant challenges due to the variability in failure modes across devices, leading to a substantial engineering burden. For instance, during an EFR qualification involving 20,000 dice, it is common to encounter approximately 200 failures. However, due to resource constraints, only a limited subset—typically around 10% (or 20 failures)—can be subjected to EFA by a small team of engineers over a two-week period. This limited sampling often results in incomplete coverage of failure modes, increasing the risk of undetected issues that could compromise device reliability.

Our research aims to develop a batch EFA approach that enables comprehensive analysis of all identified failures within a constrained timeframe, thereby enhancing the reliability assessment of semiconductor devices without being hindered by the quantity of failures.

II. Methodology and Results:

This section outlines the systematic approach employed in our study to enhance EFA for semiconductor devices. The methodology encompasses several key processes in the test program development and also the data processing script: Failure inputs, Failure die matching, Worst Word Line selection for Erase failure, Leakage Detection, the respective EFA flows for different failures and the data visualization. Each step is designed to optimize the identification and analysis of failure modes, ensuring comprehensive coverage and efficient resource utilization.

Failure inputs: User can use a config file to input all the failure information that needs FA analysis, shown is Table.1.

Respective EFA flows: Figure.1 presents that for program failures, using the input data from the die, block, and word line (WL) allows for reprogramming and the collection of status, Failure Bit Count (FBC), cell threshold voltage (V_t), and leakage information. For failures during erase, it is crucial to first identify the worst WL and then conduct the same operations as for program failures. For read failures, to preserve the incoming failure data, reprogramming is not performed; instead, only V_t and FBC data are collected.

Failure die matching: The die ID returned by the test program is compared with Failure input information defined in the config file. This comparison allows EFA to be conducted solely on the selected failing Die/Block although all Duts run at the same time (shown in Figure. 2). Reduce data volume and shorten testing time by retaining only essential failure analysis information.

Leakage Detection: We propose developing capabilities to transfer leak detection scripts from manual testing machines with small sample sizes to automated testing platforms capable of handling large sample volumes at the same time. The current leakage detection system can rapidly operate on hundreds of dies within one minute, significantly enhancing efficiency in failure analysis.

Data visualization: We need to transform the data from hundreds of received dies into a visual format that enables users to quickly grasp the failure information for each die. This will facilitate the identification of failure patterns and allow for the rapid detection of failures related to process or trim.

III. Conclusion:

The new Failure Analysis (FA) methodology as shown in Figure. 3 has been widely applied in the testing of DPPM. It enables the collection of diverse failure information during the early stages of development, establishing a robust failure information database for each generation. By integrating contemporary artificial intelligence techniques, this approach facilitates the rapid identification of issues in early process and trim development. Consequently, it provides timely solutions, accelerating the transition of products into mass production. Such insights can be communicated to the process and device teams for targeted improvements, ultimately accelerating the time-to-market for the product.

Failure Type	Cycle	Die_ID	Block	WordLine	String
Erase fail	C1	X1_Y1_Z1	M1	N1	P1
Program fail	C2	X2_Y2_Z2	M2	N2	P2
Read fail	C3	X3_Y3_Z3	M3	N3	P3
Erase fail	C4	X4_Y4_Z4	M4	N4	P4
Program fail	C5	X1_Y1_Z1	M5	N5	P5
Read fail	C6	X2_Y2_Z2	M6	N6	P6

Table.1 Input failure information for FA.

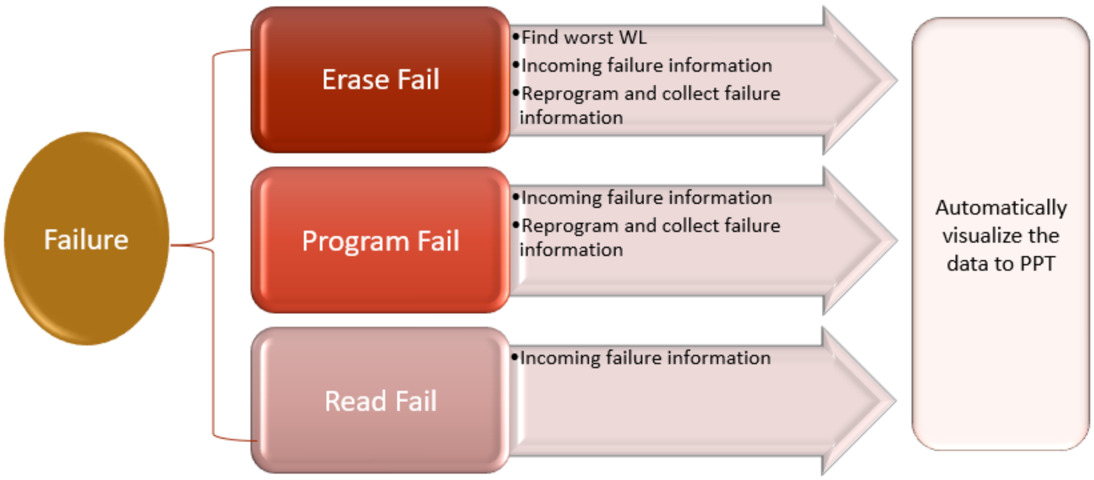

Figure.1 Respective EFA flows for different failures.

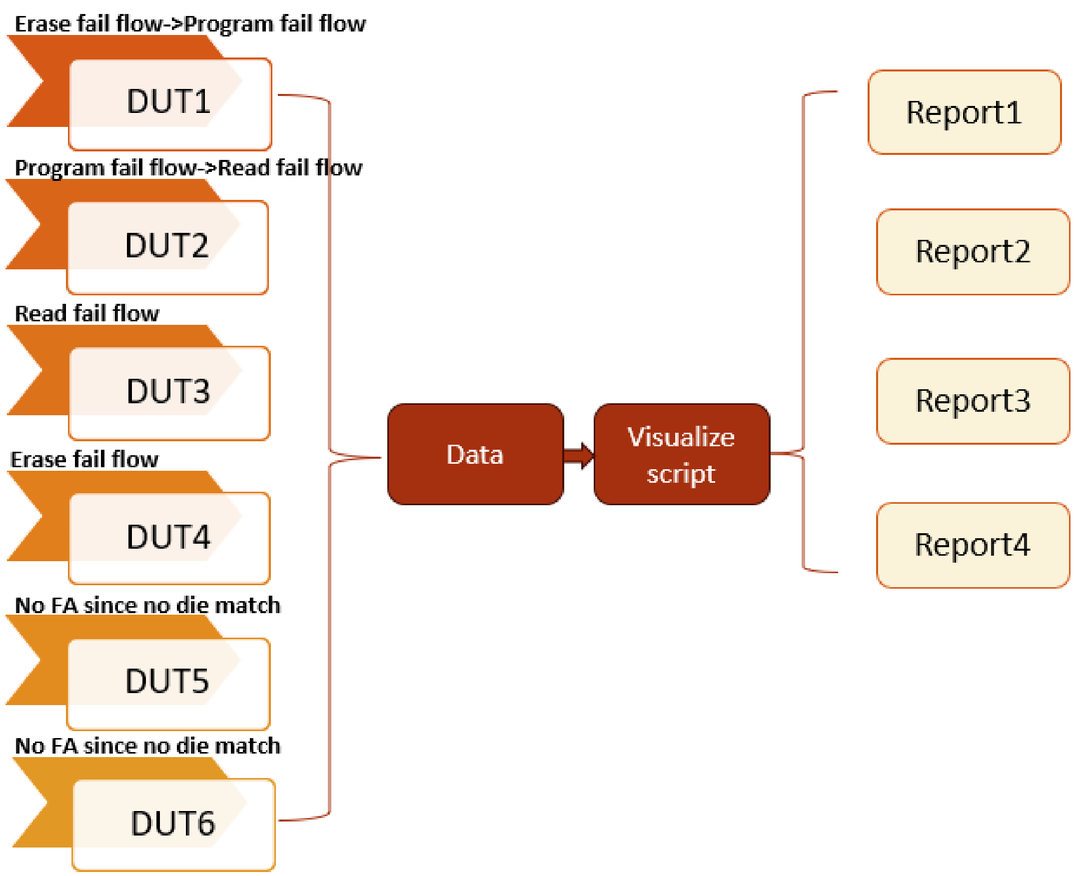

Figure. 2 Failure die matching to run different flow on different die.

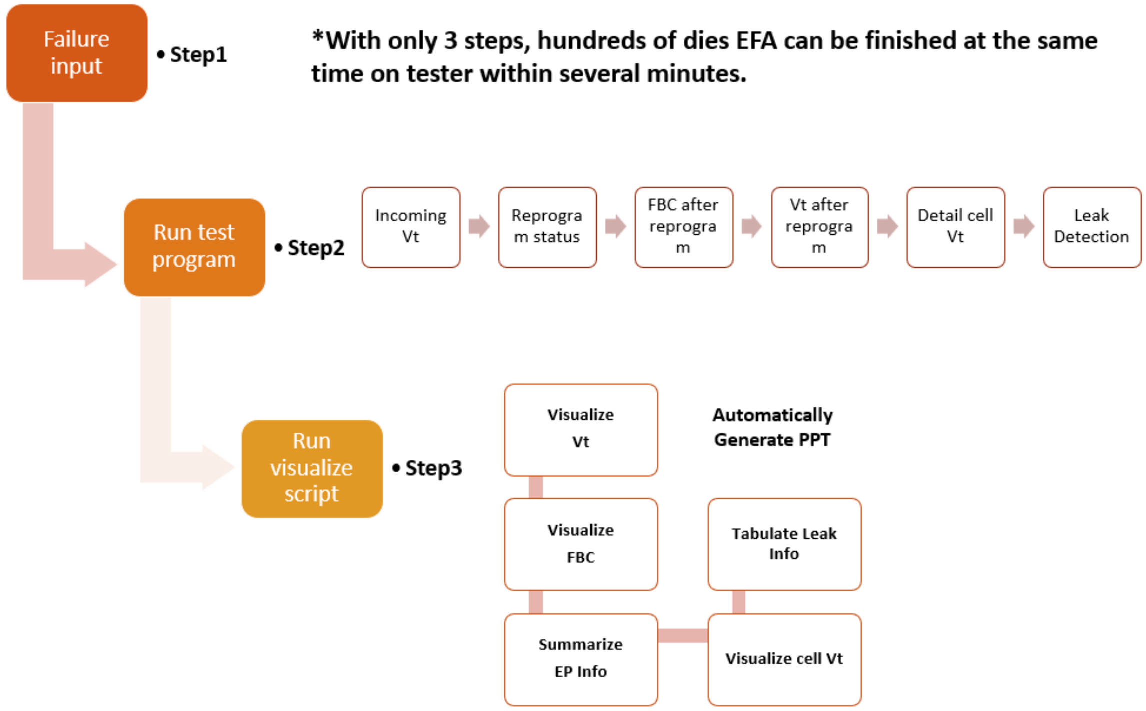

Figure. 3 The Highly Efficient Auto Batch EFA System is capable of managing hundreds of failures within a single hour, with a comprehensive PPT report generated promptly.