Navigating the challenges of Physical Verification in 3DICs: From 2D to 3D solutions

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Abstract

This paper addresses key challenges in 3DIC physical signoff verification (PV), including heterogeneous semiconductor die stacking, Through-Silicon Via (TSV), interposer complexity and Electrostatic Discharge (ESD) signoff. These factors strain traditional Electronic Design Automation (EDA) tools and necessitate new signoff verification methodologies. We present Marvell's approach to overcoming these limitations through advanced signoff techniques, enhanced automation, and shift-left debugging for early-stage verification strategies. This methodology enables scalable and efficient signoff across both 2.5D and 3D chiplet designs.

Introduction

The advancement of semiconductor technology has led to the rise of 3D Integrated Circuits (3DICs), which offer significant improvements in performance, power efficiency, and area (PPA) compared to traditional 2D designs. By vertically stacking multiple semiconductor dies, 3DICs achieve higher integration density, shorter interconnect lengths, and increased bandwidth—making them ideal for high-performance computing, AI accelerators, and mobile applications.

However, this architectural shift introduces a new set of challenges in physical signoff verification (PV). Unlike conventional 2D ICs, 3DICs integrate heterogeneous semiconductor dies, often fabricated using different process nodes, technologies, and even foundries. This complexity complicates traditional signoff verification flows, which are not equipped to handle the intricacies of Through-Silicon Vias (TSVs), micro-bumps, interposer (silicon bridge) routing, and semiconductor die-to-die alignment.

As the industry transitions from 2D to 3D design paradigms, there is an urgent need to rethink and adapt physical signoff verification (PV) methodologies. This paper explores the key challenges in 3DIC physical signoff verification (PV) and presents emerging solutions and frameworks designed to address these challenges efficiently and reliably.

Problem Statement

As semiconductor designs evolve toward 3D integration to meet increasing demands for performance and density, traditional physical signoff verification (PV) methodologies face significant limitations. The transition from 2D to 3DICs introduces complex challenges such as multi-semiconductor die-to-die alignment, heterogeneous process technologies, inter-semiconductor die connectivity using Through-Silicon Via (TSV)s and micro-bumps, and cross-foundry, cross-nodes design rule compliance. Existing signoff verification flows—primarily optimized for planar designs—struggle to scale and adapt to the intricacies of vertical stacking and interposer silicon bridge-based architectures.

This paper highlights the critical need for robust, scalable, and efficient physical signoff verification frameworks tailored to the unique demands of 3DICs. It examines the limitations of current 2D-centric approaches and explores emerging solutions that enable accurate, high-throughput signoff verification across multiple semiconductor dies and integration schemes.

3DIC Physical Verification Requirements

To address the unique challenges introduced by 3D integration, this paper presents a comprehensive physical signoff verification methodology tailored for 3DIC designs. The methodology spans four critical domains: Design Rule Checking (DRC), enhanced Antenna effect check (ANT) accounting for multi-die scenarios, Layout Versus Schematic (LVS), and Electrostatic Discharge (ESD) signoff verification using Programmable Electrical Rule Check (PERC).

1. 3DIC Physical Verification Flow Overview

Marvell Multi-Die Physical Verification flow integrates single semiconductor die, package interconnect and encapsulation, and multi-semiconductor die signoff verification into a unified methodology that supports heterogeneous integration and shift-left debugging for early-stage verification. As illustrated in **Figure 1**, the verification process begins with the independent signoff each signle Die, shown in the upper left quadrant. This includes a range of components such as system-on-chip (SoC) chiplets, High Bandwidth Memory (HBM), and dummy decoupling capacitor dies. Each die undergoes comprehensive validation using multi-DRC (Design Rule Check), antenna effect analysis (ANT), Layout Versus Schematic (LVS) comparison, and Electrostatic Discharge (ESD) checks. The methodology is inherently scalable, accommodating any number of dies within a chiplet-based architecture. The second stage, depicted in the bottom left quadrant of **Figure 1,** focus on the signoff of the package interposer and substrate. This phase ensures the integrity of interconnects and compliance with encapsulation-level design constrains. The final stage, shown in the upper right quadrant, involves the verification of the complete 3D stack. It leverages 3DBlox™ standard for 3D layout representation for layout assembly and netlist for logical inter-die connectivity representation conversion. This culminates in a 3DSTACK inter-die connectivity validation check to ensure inter-semiconductor die connectivity and die-to-die alignment. This scalable approach ensures signoff quality across all integration levels and enables robust, high-throughput signoff verification for advanced chiplet and 3DIC designs.

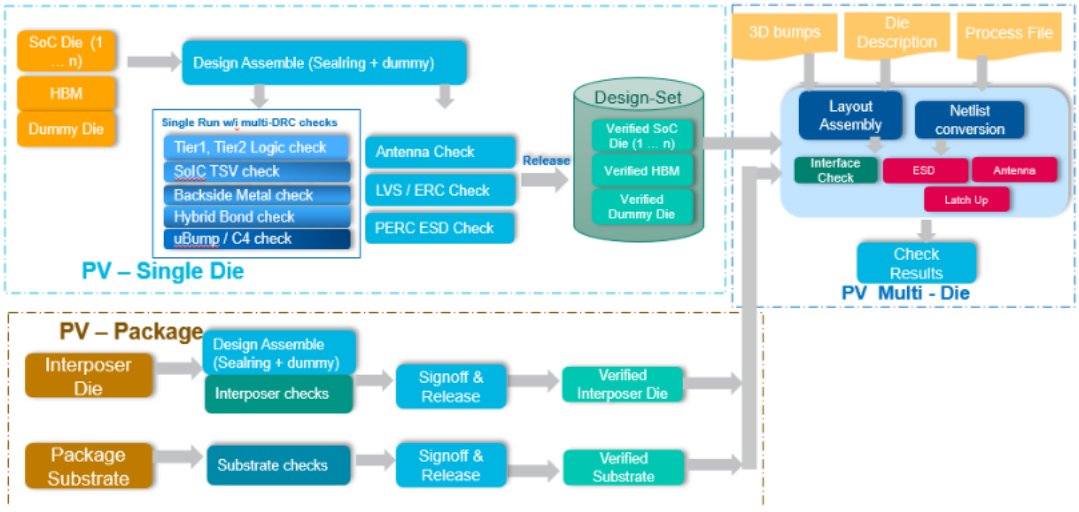

Figure 1 3DIC Physical Verification Flow Overview

In 3D systems-in-package, checking for the antenna effect becomes more complicated. The antenna effect, also known as Plasma Induced Damage (PID), occurs during the manufacturing

process when charge accumulates on metal interconnects and discharges through sensitive gate oxides, potentially damaging MOSFETs. Traditional DRC includes antenna rules that check the area ratio between metal layers and gate layers, essential for ensuring manufacturability and reliability. Antenna rules are layer-specific and may include exceptions or waivers based on protection diodes or connectivity. In multi-chiplet packages, antenna effect checking becomes more complex due to multiple power domains, isolated wells, and cross-die connectivity. Advanced path-based antenna verification is needed to handle these scenarios.

2. Seal Ring Methodology for 3DIC

A key enhancement in Marvell's 3DIC physical signoff verification (PV) flow is the automated insertion of seal rings for hybrid bonding interfaces, ensuring compliance with foundry-specific requirements for manufacturability and reliability. Seal rings provide mechanical protection during wafer dicing and provide environmental isolation, blocking moisture and contaminants from entering the chip under high humidity and temperature conditions. Seal rings are added based on chip dimensions after semiconductor die assembly and Design Rule Checking (DRC) clearance, and critically, their insertion does not introduce any Design Rule Checking (DRC) violations, preserving a clean signoff verification state. However, because seal rings for hybrid bonding interfaces are inserted outside the place-and-route (PnR) tool and post-assembly, they are not visible within the PnR environment, which prevents dummy Hybrid Bond Pad (HBP) assignment. To address this, the seal ring insertion flow has been enhanced to automatically generate dummy HBPs with full Design Rule Checking compliance. **Figure 2** illustrates the placement of HBP on TSMC SoIC™ (System-on-Integrated-Chip) Tier1 (T1) die, along with the projected HBP locations from the Tier2 (T2) die into T1. The automatically inserted dummy HBPs over the seal rings of both T1 and T2 dies enable interface alignment checks during chip and stack floorplanning. Additionally, the BSAM (Chip-on-Wafer Overlap Mark), placed by the PnR tool, provides a reference for alignment accuracy and process quality.

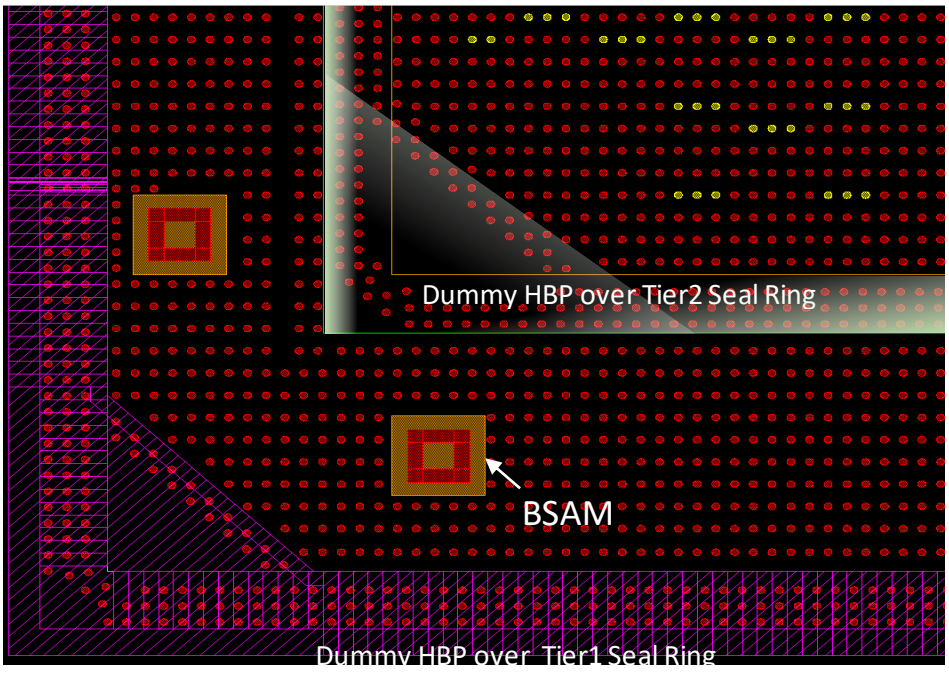

Figure 2: Seal ring with Dummy Hybrid Bond Pad

3. **Design Rule Checking (DRC) at Multiple Levels to enable TSMC 3DIC integration**
   Figure 3 shows a 3DIC system in package. There are three SoCs, with chip1 and chip2 vertically stacked on chip 3. High Bandwidth Memory (HBM) is integrated with the 3D stacked chips on an interposer, which is then assembled on the package substrate. Die-level Design Rule Checking (DRC) has been integrated into a single run, unifying multiple checks such as Logic, TSMC SoIC™ Through-Silicon Via (TSV), backside metal, hybrid bond, and micro-bump into one runset. This integration allows all checks to be performed in one shot and provides a flexible run mode to enable floorplan design rules at the early design stage. Interposer package Design Rule Checking supports multiple variants of CoWoS (Chip on Wafer on Substrate) packages with package substrate check enablement. Die-package co-Design Rule Checking brings chiplet dimension rules, including width, length, area, and aspect ratio, into intra-silicon Design Rule Checking.

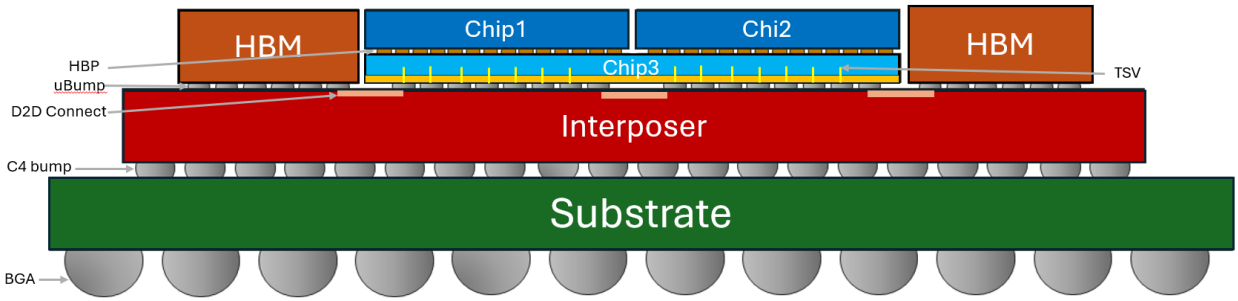

Figure 3: TSMC 3D Integration

4. **Layout Versus Schematic (LVS) and Connectivity Verification**
   In 3DICs, especially in TSMC SOIC™ Face-to-Face (F2F) configurations, ensuring correct semiconductor die-to-semiconductor die inter-die connectivity is critical. The enhanced Layout Versus Schematic (LVS) methodology includes net matching across dies, ensuring that corresponding hybrid bond bumps on each semiconductor die are connected to the same logical net. Additionally, it involves system-level netlist comparison, which entails assembling the full 3D layout and comparing the extracted netlist, or logical inter-die connectivity representation, against the top-level system netlist to validate inter-die connectivity. Finally, the methodology includes die alignment and overlap checks, verifying that overlapping hybrid bond bumps are correctly aligned and electrically consistent, as shown in **Figure 4** and **Figure 5**.

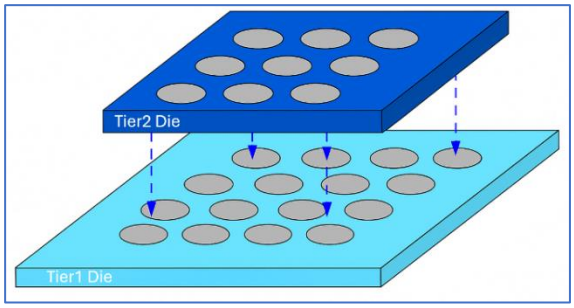

Figure 4: Face-to-Face Stacked Die with HBP overlapping

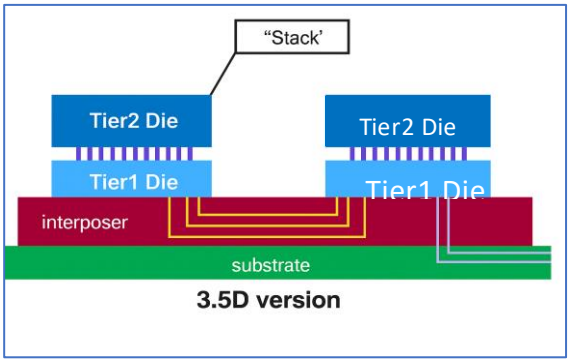

Figure 5: Face-to-Face Stacked Die.

5. Electrostatic Discharge (ESD) Verification at the 3D Level

ESD sign-off verification in 3DIC designs is critical to ensuring circuit reliability and manufacturing yield. Traditionally, ESD verification has been performed at the die level in a 2D context, where each die is analyzed as a standalone entity. In this work, we extend the ESD verification methodology to address the unique challenges of 3D integration, with a particular focus on TSMC SoIC™ Face-to-Face (F2F) die stacking.
Figure 6 illustrates a cross-sectional view of two dies from different technology nodes stacked F2F using TSMC SoIC™ technology. Communication between the dies occurs through HBPs. Each HBP is protected by a lightweight ESD I/O circuit, which is a simplified version of the traditional GPIO (General-Purpose Input/Output) ESD protection structure. For HBPs on the top die that interface with external I/Os through the package, full GPIO-based ESD protection is required. Additionally, there are feedthrough nets that traverse the bottom die via TSVs and connect directly to the top die, either to power clamps or GPIO ESD cells. These nets must be carefully designed to ensure robust connectivity to ESD protection devices. To comprehensively address these diverse ESD scenarios in 3D designs, we exercise an enhanced verification methodology that incorporates six dedicated ESD checks using Programmable Electrical Rule Check tailored for 3D integration:

Check 1: Connectivity from one hybrid bond to its facing counterpart, which is the connectivity from Top die (T1) to bottom die (T2) in **Figure 6**.
Check 2: Micro-bump die-to-die signal pad routing from the backside to T1 and continuing into T2 semiconductor dies in **Figure 6**.
Check 3: IO signal pad directly connected from the backside only to T2 General-Purpose Input/Output, labeled GPIO in **Figure 6**.
Check 4: Power/Ground (P/G) bump directly connected from the backside to T2 power clamp cells, shown in **Figure 6**.
Check 5: Power/Ground (P/G) bump connected from the backside to both T1 and T2 power clamps (PCs), show in **Figure 6**.
Check 6: Power/Ground (P/G) bump connected exclusively to the T1 bottom semiconductor die, shown in **Figure 6**.

These six checks encompass Topological checks to identify the ESD protection circuits, Point-to-point (P2P) checks to measure the resistance from the ball to the ESD protection, and Current Density (CD) checks to ensure there is sufficient metal to withstand lifetime ESD current. The checks can be coded in a tool such as Siemens Calibre® PERC™ or Synopsys IC Validator™.

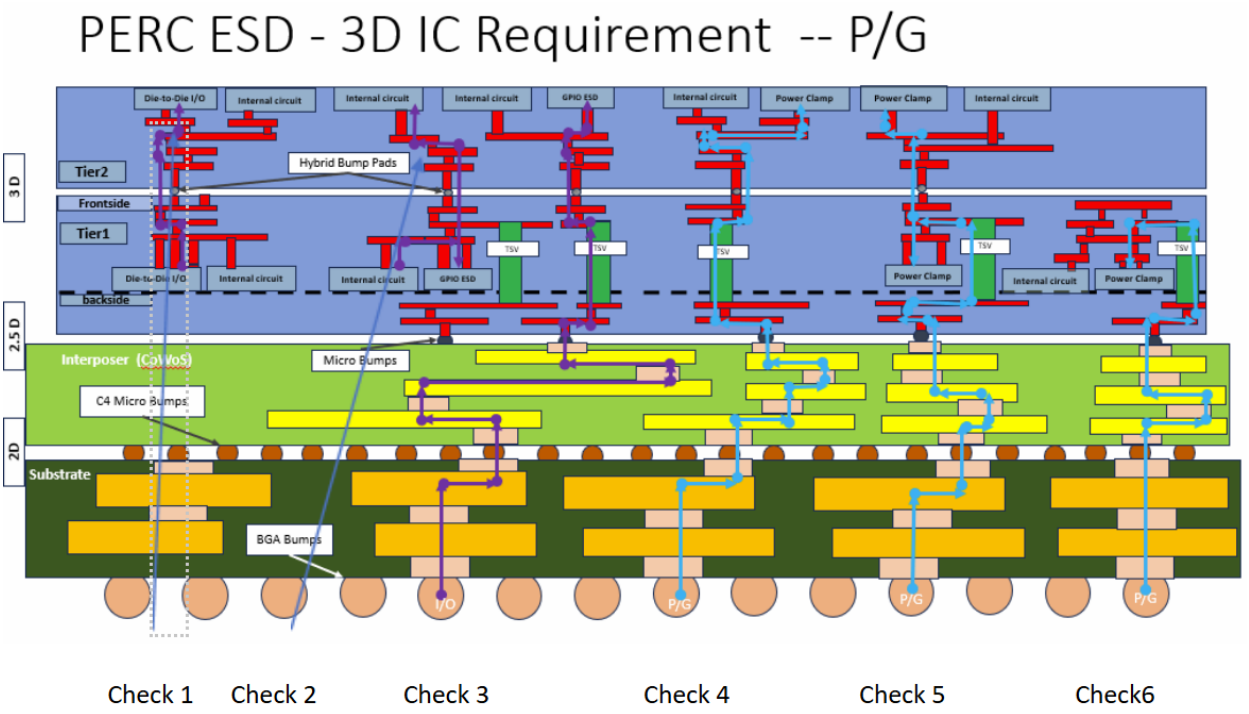

Figure 6: 3D ESD Electrical Rule Check

To ensure comprehensive protection across the entire die-to-die stack, ESD verification is extended to include both the substrate and logic dies. This involves measuring the point-to-point resistance from the Ball Grid Array (BGA) solder balls to the final ESD protection cells located on either the top or bottom die. **Figure 6** illustrates a configuration with multiple die stacks mounted on an interposer.
This holistic methodology validates ESD protection across all critical paths, including vertical and lateral interconnects, as well as across multiple SoC dies and package layers. By doing so, it ensures robust ESD coverage for complex 3DIC systems.

ESD Electrical Validation Checking Results

Figure 7 shows TSMC SoIC™ design ESD signoff verification. Once the inter-die connectivity has been established through hybrid bond pad, we will proceed to check the correctness and adequacy of ESD solution through the BGA solder balls of the package. The design in **Figure 7** represented two 3D-stacked dies on top of package substate.

Figure 7 also illustrates the flight lines from the GND ESD pad to the core voltage power clamp, with violations highlighted in the Calibre® RVE window. These flight lines help designers quickly identify the locations of the GND pad and the core clamp, making problem diagnosis and resolution more efficient. For example, the resistance rule requires a value below 0.1 Ω. The tool reports the actual measured resistance between the two clamps, enabling designers to compare it against the rule. Based on this comparison, engineers can assess the severity of the violation and implement corrective actions, such as optimizing the layout to reduce resistance.

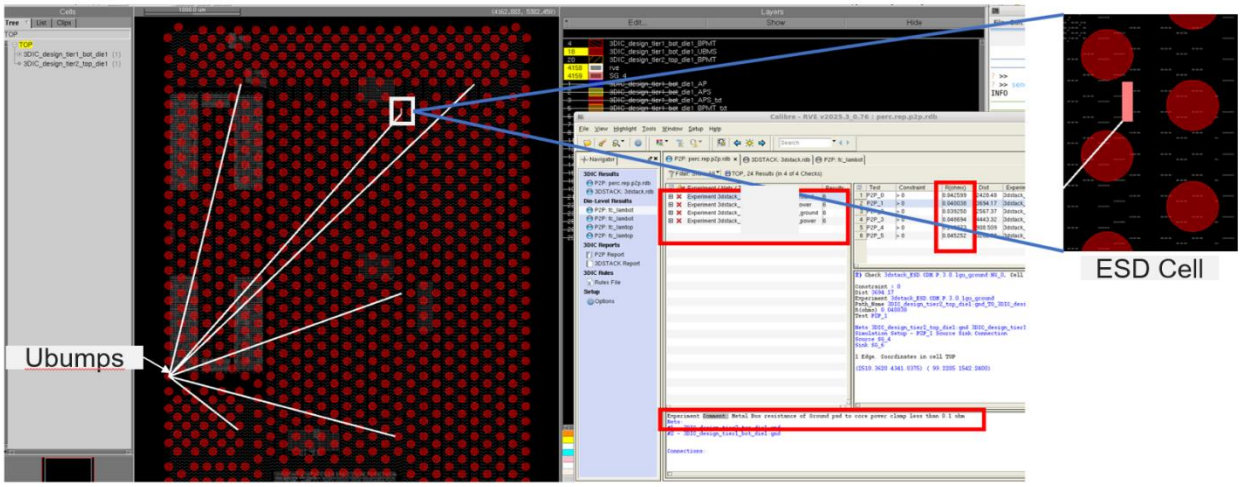

Figure 7: TSMC SoIC™ design ESD signoff verification strategy

Figure 8 illustrates the connectivity from the BGA ball on the backside of the package substrate, to the bottom semiconductor die and further up to the top semiconductor die. The verification process calculates the resistance path starting from the backside C4 bump all the way to the power clamp (ESD protection circuit, indicated by the pin in **Figure 8**) located on the top die. The design analyzed in **Figure 8** contains two pairs of 3D-stacked SoC dies on an interposer on substrate, which allows multiple parallel paths between the two die stacks. This is the configuration which was illustrated in **Figure 5**.

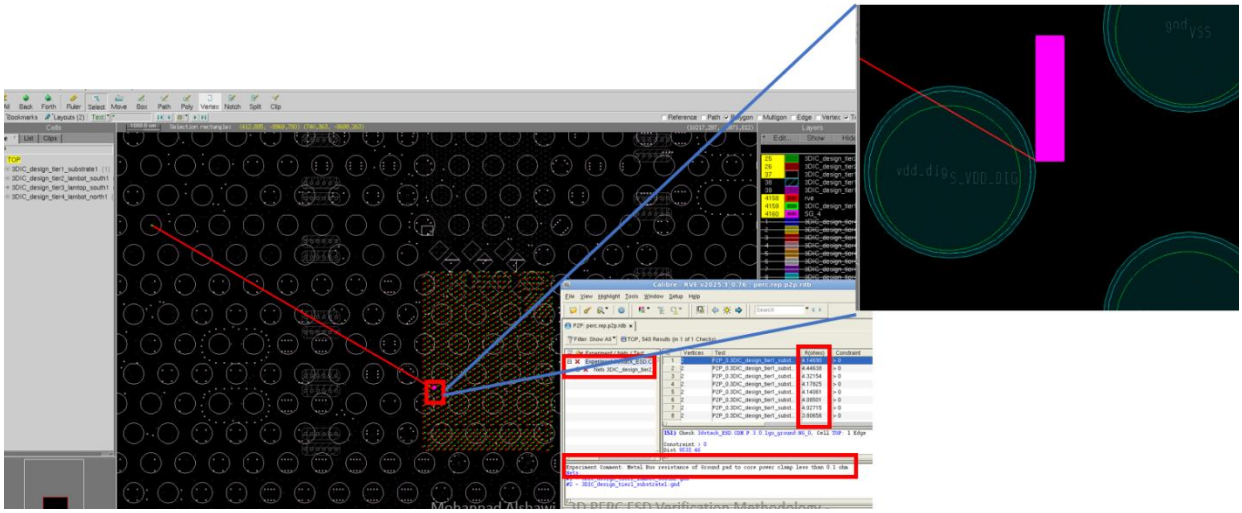

Figure 8: ESD P2P Resistance Result from C4 bump to Power clamp on top die

Conclusions:

As semiconductor architectures evolve from planar 2D designs to vertically integrated 3DICs, the complexity of physical verification (PV) grows exponentially. Traditional signoff methodologies are no longer sufficient to address the challenges posed by heterogeneous die stacking, TSVs, interposers, and advanced bonding technologies. This paper presents a comprehensive and scalable PV framework

tailored for 3DICs, integrating multi-level DRC, LVS, antenna checks, and 3D-aware ESD verification using advanced tools like Siemens Calibre® PERC™, Synopsys IC Validator™.

Marvell's approach—anchored in shift-left verification, automation, and standards like 3DBlox™—enables early detection of design issues, robust die-to-die connectivity validation, and reliable ESD protection across complex stacks. By unifying die-level, package-level, and stack-level verification into a cohesive flow, this methodology ensures manufacturability, reliability, and signoff integrity for next-generation chiplet and 3DIC systems.

Looking ahead, future research will focus on 3D antenna checks by extracting full 3D connectivity, modeling charge accumulation across dies in vertically stacked configurations. Additionally, advanced ESD modeling techniques are needed to simulate dynamic discharge paths across hybrid bonds, TSVs, and package layers, ensuring robust protection in increasingly dense and heterogeneous 3DIC environments. These innovations will be critical to sustaining the reliability and scalability of future semiconductor systems.

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