

Scaling Electro-Optical Test and Reliability Validation of Silicon Photonics for AI and Hyperscale Data Centers

Tala Sidawi
Ayar Labs
San Jose, California

Annie Hsieh
Ayar Labs
San Jose, California

Đorđe Gluhović
Ayar Labs
San Jose, California

Abstract—The explosive growth of generative AI is driving unprecedented demands on bandwidth, power efficiency, and system scalability, exposing fundamental limitations of conventional electrical interconnects. Ayar Labs is addressing these challenges with a leading-edge silicon photonics (SiPh) co-packaged optical (CPO) platform that enables high-bandwidth, energy-efficient data movement for next-generation AI infrastructure. By integrating photonics and electronics within a unified package, optical I/O overcomes the power and bandwidth-density constraints of electrical interconnects, enabling continued scaling of AI training and inference systems. With technologies such as dense wavelength division multiplexing (DWDM), micro ring-based optical modulation, and ultra-high-density optical port density, optical I/O represents a foundational technology for future hyperscale AI systems.

However, widespread deployment of CPO technology requires more than device-level innovation; it demands manufacturing-ready solutions that deliver high yield, reliability, testability, and scalability at volume. The tightly coupled nature of electro-optical devices, advanced packaging, and system integration introduces new challenges in process control, test coverage, automation, and reliability qualification. Rapid design iterations further require scalable development methodologies capable of bridging the gap between R&D laboratory demonstrations and high-volume manufacturing.

This paper presents a comprehensive high volume manufacturing test technology and reliability framework. It includes automated test architectures, high-throughput reliability testing methodologies, electro-optical wafer sort (EOWS), packaged part qualification strategies, and data-driven process monitoring for volume production. Experimental results demonstrate how automation, scalable test infrastructure, and reliability hardware development improve repeatability, accelerate product qualification, reduce operational complexity, and establish the foundation required for hyperscale deployment of optical I/O. The work provides a practical framework for transitioning CPO from emerging technology to production-ready infrastructure capable of supporting the next generation of AI computing systems.

I. INTRODUCTION

Unprecedented computational demands of modern AI have outpaced Moore’s law and exposed the weaknesses in existing ecosystems that are incapable of satisfying sub-pJ/bit energy efficiencies at terabit data rates [1], [2]. Silicon photonics promises to resolve the copper-interconnect bottleneck, delivering high bandwidth and low latency state-of-the-art at the inflection point of tera-scale computing applications. The transition to an end-to-end optical PHY leverages mature,

well-developed CMOS infrastructure and packaging techniques for standard silicon chips [1], [3]–[9]. This reduces initial fabrication costs and ultimately paves the way for SiPh commercialization. At Ayar Labs, the TeraPHY™ optical engine is a CPO architecture that uses DWDM-spaced micro-ring modulators for electro-optical signal conversion paired with resonant photodetectors at the receiver, achieving speeds up to Tbps [10]. Ring locking control circuits drive signal translation across parallel macros, enabling temperature-robust systems for wavelength-sensitive devices. Powered by an OCI-MSA-compatible SuperNova™ external laser small form factor pluggable (ELSFP), the TeraPHY optical engine provides ubiquitous GPU-to-GPU communication at 10x higher bandwidth than conventional copper and pluggable optics, with a 2 Tbps/mm shoreline bandwidth density and exceptional bit error rate (BER).

At the heart of SiPh is the photonic integrated circuit (PIC), responsible for the manipulation, modulation, and detection of light in sub-micrometer waveguides enabled by the high refractive index contrast of silicon-on-insulator (SOI) technology [3], [6], [11]. Complex PICs are designed using the building blocks of optical components like grating couplers, waveguides, and wavelength filters [3], [12]–[14]. These structures have improved significantly over the last decade due to the development of SiPh process design kits (PDK) offered by foundries to standardize and maximize individual device performance and serve as a starting point for design applications [3]. Fabrication techniques have followed suit with the development of TSMC’s Compact-Universal-Photonic-Engine (COUPE), an integration technology for optical engines (EIC-PIC) compatible with host ASICs for high quality CPO [15]–[17]. Most importantly, the COUPE solution is designed to optimize high yield and low insertion loss for grating and edge couplers that meets wafer level system integration (WLSI) requirements [17]. This is especially significant as we approach the challenge of product scalability. As SiPh technology evolves, so too must the post-silicon test, validation, and reliability infrastructures to meet the demands of industrial production.

Minor issues in low-volume applications inevitably become critical roadblockers at the level of high-volume manufacturing (HVM). Passive photonic structures that require nanometer-

scale tolerances are highly sensitive to process-induced variability (e.g., waveguide fabrication, polarization sensitive components, precise matching of center wavelength and waveguide propagation constants, wavelength filter efficiency) and compensate using active structures to meet exact specs during operation [11], [18]–[21]. Wavelength, temperature, and electrical carrier dependent design considerations must match accurate simulation behavior of the material refractive index for photonic circuits to overcome these challenges [18]. Intricate devices are susceptible to detuning without local temperature control accuracy better than 0.1 K, corresponding to wavelength shifts of 10 pm [22], [23]. 1 nm variations in height and width during fabrication correspond to a 1 nm shift in center wavelength [18]. Despite these challenges, high yield and fabrication uniformity are critical to low-cost silicon technology [24]. If they cannot be solved, deviations must be well understood.

The ultimate goal is high-throughput optical testing without sacrificing yield, reliability, testability, and performance at volume. Without established methods or integrated solutions, continuous process automation and rapid design iterations require specialized testers and test structures [14]. Successful in-line optical test systems (ILOTS) accurately monitor the process-line health and the quality of the communication link with maximum precision and speed [14], [25], [26]. Design optimization is a focus of modern work on SiPh testing [27]. Innovative solutions leverage pre-existing wafer dicing trenches for edge coupling to maintain low cost sub-micron optical fiber alignment [28], [29]. Packaged SiPh circuits add significant cost over raw wafer circuits [26]. Therefore, reliability validation must manage packaged part qualification while maintaining high-throughput results that comply with GR-468 and the newly released JESD264 standards required by customers [30], [31]. For CPO, the ideal optical reliability level is better than or equal to the failure rate of the attached ASIC [1]. In this paper, we present an architecture for custom, automated electro-optical SiPh wafer test and packaged part reliability stations and discuss key future hardware development challenges. Experimental results demonstrate the improved stations’ success in delivering high-sample-size results, with live plotting of spatial heatmaps over 1000-hour stress tests followed by root-cause investigation of unexpected error sources during wafer level reliability stress.

II. AUTOMATED ELECTRO-OPTICAL WAFER TEST ARCHITECTURE

In the semiconductor industry, traditional high-volume test solutions use electrical automated test equipment (ATE) on a probe system, with a probe card that interfaces with the wafer device under test (DUT). On the other hand, SiPh electro-optical wafer level tests have been only implemented on engineering test platforms over the past few decades without a full turnkey solution in the market. Engineering probe systems support hardware customization to meet a wide range of test requirements, from device characterization to low-volume production test. Until a fully automated HVM test cell is

available, SiPh wafer level platforms still require a custom equipment ecosystem to meet the increasing demands of PIC testing in production environments.

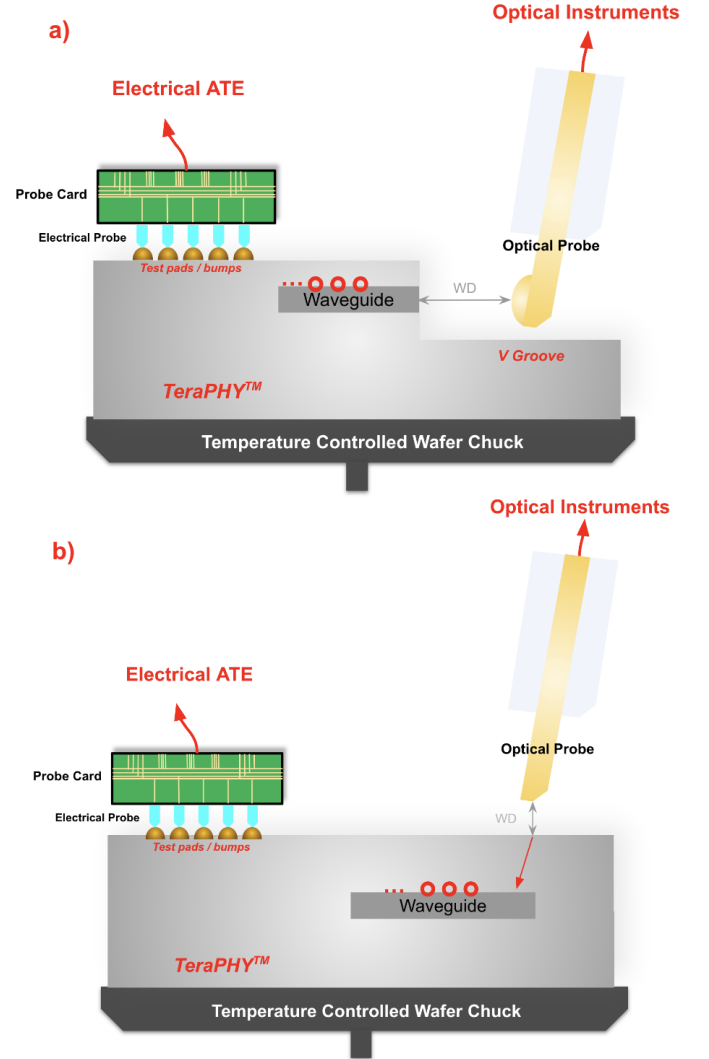


Fig. 1: Wafer level test schematic using (a) an edge coupling method and (b) a surface coupling method.

A. Test Architecture

Successful test architecture produces accurate, repeatable measurement results to evaluate the actual performance of the chip design. An automated SiPh test cell consists of a wafer probe system, ATE, optical instrumentation, optical probes, and a probe card interfacing the wafer DUT (Fig. 1) [32], [33]. A wafer probe system allows for full automation of wafer and probe movement during the test process from die-to-die and wafer-to-wafer. Precise mechanical movement for electrical and optical probing is essential for test accuracy and repeatability. ATE and optical instrumentation send and receive stable signals to and from the DUT through the probes. A centralized controller workstation controls all the subsystems in the test cell for test program development. The test program

is the heart of the test measurement because it defines the test flow, test recipe, hardware configuration, test method, and datalog. Test flow defines the test process for optical coupling setup sequence, probe-to-pad alignment, and all test cases for the measurement based on the test plan of the device. Test conditions and requirements are specified by the test recipe and hardware configuration. The test method defines the execution of the test routine and the data of interest during the measurement, then constructs the datalog for binning and device disposition decisions.

B. Test Process and Test Time Challenges

Typical test flow begins with wafer loading and alignment, probe alignment, first light search, optical alignment, and finally executes test measurements in sequence. The active alignment of the optical probe is key to the performance of optical coupling. To achieve maximum coupling efficiency, the optical probe measures a spatial power map to target the position with the highest optical throughput. Different coupling methods also have different optical alignment requirements. Grating couplers channel the light to the waveguide on top of the wafer surface and are sensitive to the optical probe angle and working distance, requiring 6-axis movement to achieve optimal coupling efficiency. Alternatively, edge couplers are less sensitive to the probe angles but are limited to movement within the sub-micron V-groove trenches on the wafer for active alignment search routine. This added optical alignment process significantly lengthens test time compared to electrical-only systems and has many opportunities for improvement in the industry without sacrificing test quality.

C. Test Software Challenges

The complex nature and difficulties of the test architecture extend into the software integration. Robust safety fencing systems that prevent collisions between hardware components and the wafer are even more challenging when mixing different subsystem hardware components from multiple vendors. The delicate balance between probe-to-wafer coupling loss and damage risk to the wafer is a trade-off of signal quality at distances as low as tens of micrometers. A safety fencing feature is imperative to mitigate this risk, requiring a well developed control software network of the fiber attached unit (FAU) control module, probe chuck control system, and camera for image processing. Additionally, there is a lack of standardized optical instrument drivers due to the highly customized optical instrument rack configuration that varies with different test requirements and test plans. This poses yet another challenge in the software development of the test program driver integration without any temporary workarounds. Optical instrument integration and electro-optical signal synchronization with the ATE is also yet to be developed. This is critical for photodiode tests or characterizations that often require triggering signals with incredibly precise timing for wavelength sweep or polarization sweep measurements. Hardware coordination is even more critical for optical high-speed signal tests like eye diagrams and bit error rate. With an asynchronous trigger, the

sampling relationship drifts and further introduces instability and jitter in the eye measurement [34].

D. Test Hardware Challenges

Hardware stability and precision of component control have reached a theoretical limit, especially as various environmental factors affect hardware performance. Due to the nature of the technology, the effect of facility vibration is unavoidable when evaluating optical coupling performance for SiPh test measurements. Vibrations of the FAU and the wafer chuck directly impact optical coupling performance into the silicon device and the signal integrity. Thermodynamic effects in the system further exacerbate these sources of error at high temperature testing conditions. Additionally, to accurately measure device performance at operating conditions, the test architecture must support the integration of high powered lasers based on the optical link budget performance [35], [36]. Laser source requirements consider all external instrumentation losses and coupling from the FAU to the DUT surface to correctly evaluate the operational nonlinear loss of the waveguide, receiver sensitivity, and device crosstalk [35]. Commercial vendors are already producing ultra-high powered lasers to address these exact optical loss challenges, significantly increasing the risk to test operator safety. To ensure ideal laser safety and test quality, fully enclosed wafer prober and optical instrument rack environments are required.

E. Test Calibration

Last but not least, optical test calibration is essential because measured optical power depends on both device performance and the test setup. Before testing, the fiber probe must be aligned to the on-wafer coupler to enable optical path calibration across the required wavelength range, input power, and polarization. A well-done calibration method reduces the effect of minute changes in input conditions, improving assessment of true insertion loss, transmission spectra, photodetector responsivity, and modulator performance for design feedback. Calibration becomes challenging as the prober moves across the wafer; changes in wafer height can alter the probe-to-wafer distance, while fiber movement can shift alignment or polarization. Connector changes, probe-tip contamination, and instrument drift introduce further variation over time. Reference structures, periodic power checks, and repeated alignment help distinguish genuine differences between devices from changes in the measurement setup, increasing consistency of results across dies, wafers, and test runs.

III. HIGH-THROUGHPUT COMPONENT RELIABILITY TESTING

A. Optical Damage

The key risks of SiPh component reliability are: (1) high optical power handling of the Si waveguide and (2) thermal tuning of the microring. Resulting material failure causes loss-of-lock, high-BER, and, when waveguide damage occurs, increased insertion loss. The goal is to quantify instantaneous damage thresholds and determine the existence of measurable

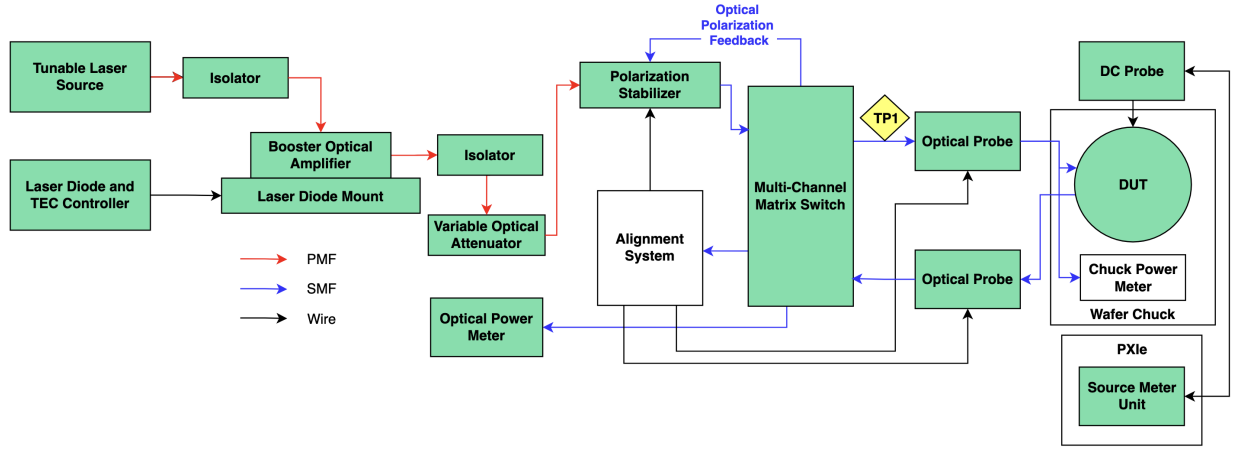


Fig. 2: Schematic diagram of wafer level optical damage using the wafer prober. The active optical train during the experiment is marked in green.

degradation for both product and test chips. If component degradation exists and can be isolated, we can build failure models to predict reliability lifetime for new device designs.

Optical damage was previously observed on low-volume packaged TeraPHY parts that affected known good die (KGD) deliverables. Alternatively, lowering the laser input power is insufficient to close the optical link. Physical failure analysis showed damage sites in the Si bus waveguide adjacent to the micro-ring modulator. Design improvements in subsequent tapeouts mitigated the high risk of operational power handling at the ring. A correlation between the optical-thermal condition and link operation suggests two possible hypotheses: (1) the local temperature of the ring depresses the damage threshold when the full data-path circuits are active and (2) ring-locking exacerbates the damage mechanism, possibly via increased internal reflection due to standing wave when on-resonance. Root cause analysis concluded that there is a possible role of limited bandgap (single-photon) absorption that can be relevant at or near expected temperatures of the ring and bus waveguides. Typically for room-temperature silicon, single-photon absorption is only relevant for wavelengths less than 1100 nm (1.1 eV). However, two-photon absorption (TPA) generates carriers that can absorb infrared light via free-carrier absorption (FCA), generating excess heat when the excited carriers relax [37]. The literature supports that the magnitude of absorption at 1300 nm at elevated temperatures is comparable to the absorption of 1100 nm light at room temperature [37]. Applying a safety margin according to the 100G CWDM4-MSA spec reduces risk, but still requires successive reliability testing on product and test chips to ensure component lifetime meets the product standard. Automation of the optical damage station has directly influenced variant downselection and supports immediate, high-throughput, high quality results required for successful design decisions.

The wafer level optical damage setup is built around a standard wafer loader and prober (Fig. 1). The electro-optical two-probe configuration is presented in Fig. 2, where a

polarization-maintaining (PM) tunable laser source is amplified by a 400 mW fiber coupled high power booster optical amplifier (BOA), providing +10 dB of gain to the laser input. To increase the signal stability of the amplified light, a variable optical attenuator (VOA) controls the loss of light after the BOA. The polarization stabilizer fixes the state of polarization (SOP) of the input light to align with the output of the DUT. Power at the DUT input (TP1) is calibrated at the point after the multi-channel matrix switch, before the optical probe. Output power is measured with an optical power meter at the end of the train. Each target test structure is swept from 8-16+ dBm and can cover 45 sites within an hour. A test runner can seamlessly switch between sweep and soak stress testing.

Calibration of the set attenuation to the desired input power does not require any station modifications using the optical switches. Insertion loss before and after TP1 was measured at a low optical power with an on-chuck power meter and is applied as fixed corrections to the generated calibration curve. The alignment system uses both electrical and optical feedback loops for precise fiber placement. The test sequence is based on a fixed input power range (sweep) or a maximum power for x hours (soak). Power output at the minimum level is measured before and after stress to confirm the presence of permanent damage. The design-of-experiments (DOE) for component optical power handling is a combination of varied active operations, case temperatures, and wafer locations, maximizing stress at all high-risk devices simultaneously while monitoring data in-situ and plotting output power during testing. Collected data is fed through the data pipeline, where material metadata is integrated from existing database infrastructure and key figures of merit are automatically extracted to produce raw, cleaned, and analyzed versions of the final data with traceability to the source. Post-stress characterization is also seamlessly integrated into the analysis pipeline for report-ready graphs at the moment of test completion. The results from the experiment tested on 30 reticles are shown in Fig. 3. The retest data in (a) did not

show any observable damage, and any drift in power was later attributed to measurable fiber drift during testing (see results in Section IV). The wafer map (b) of the checkerboard tested reticles does not show any spatial trend when scaled to output power below the nonlinear loss threshold.

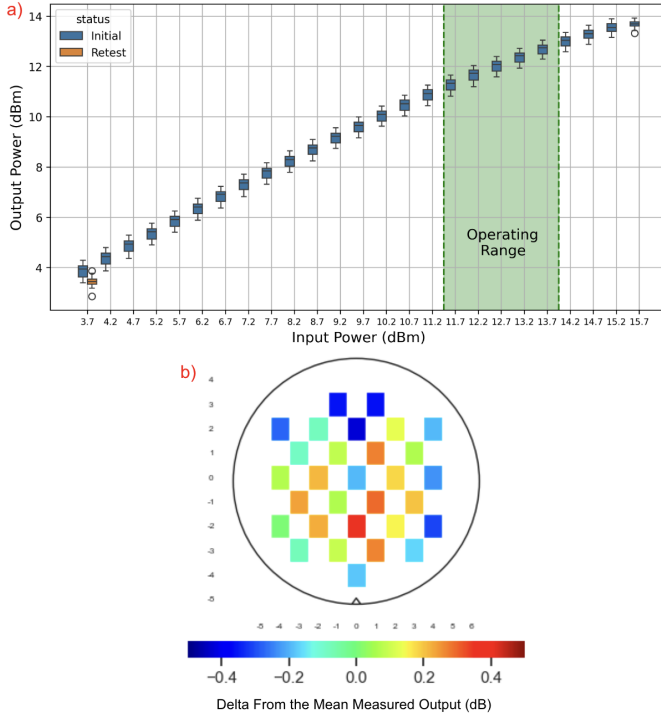


Fig. 3: Experimental results from the optical damage reliability station (a) input vs output power of test structure retested at low power (b) wafer reticle map of the output power of each test structure scaled as the delta from the mean of the dataset.

B. Heater Reliability

Ni-Si microheaters consistently fail due to electromigration in the direction of current at high temperatures, where “hot spot” points on the heater ring are void of metal, increasing resistance and creating a positive feedback loop of runaway local temperature as excess heat is generated at the points of failure. Literature values for activation energy (E_a) and current density exponent (n) of Ni-Si electromigration are $E_a = 1.71$ eV and $n = 2.01$ [38]. The relationship between electromigration and frequency on metal resistors shows that the reversal of current in a copper interconnect also reverses the direction of electromigration diffusion via self-healing. Supporting literature agrees that the alternating current exponentially increases the median time to failure compared to direct current at the same frequency and asymptotes at the lifetime threshold, where the interaction between electromigration and thermal migration degrades the material faster than the self-healing effect [39]. Advancement in the overall understanding of the failure mode of electromigration has resonated well for following chips, directly contributing to improved heater performance and lifetime with each iteration.

Automation of the heater reliability station has allowed for advanced analysis and risk assessment of heater designs during active tapeouts.

The heater reliability station is a low-cost, rack-integrated solution with a temperature controlled socket on an internally developed validation board with the capability of stressing 64 heater devices per board on 18 total stations across 3 racks. Test DOEs are based on estimated heater temperature during stress to target Mean-Time-To-Failure (MTTF) of 24/72/150/500/1000 hours. Priority is given to POR heater designs until a sufficient sample size is completed for the final report. Design variants on test chips are run at low volume to observe experimental response to stress and uncover potential failure modes outside of electromigration. Each individual device is monitored in real time during stress using a Grafana dashboard, where heater current and chip temperature telemetry are written to a prometheus file and scraped by a Grafana exporter. The resultant graph, shown in Fig. 4, is a spatial map of heater current degradation over the accelerated stress lifetime of 128 simultaneous devices, where each TX or RX device is represented in a single row. After stress



Fig. 4: Real-time current monitoring dashboard of heater degradation on a variant test chip using Grafana heatmaps. Colors are scaled from 4.5 - 2 mA (green to red). Each macro has 8 devices. Each row represents a single heater on the DUT.

completion, the new failure data is fed through an automated FIT model flow (Fig. 5) that begins with extracting the Time-to-Failure (TTF) for each device based on a 15% decrease from the initial current reading. The TTF data is then fitted with a two-parameter Lognormal distribution (μ, σ) and plotted on a probability CDF to find the MTTF. Absolute heater temperature for each MTTF condition is calculated using figures of merit collected at the wafer level to produce an Arrhenius plot of MTTF versus $\frac{1}{kT}$ that can be fitted with a linear regression to get the activation energy of the material. FIT over a lifetime T is the average of instantaneous $fit(t)$ at a given operating condition, where integrating from 0 to

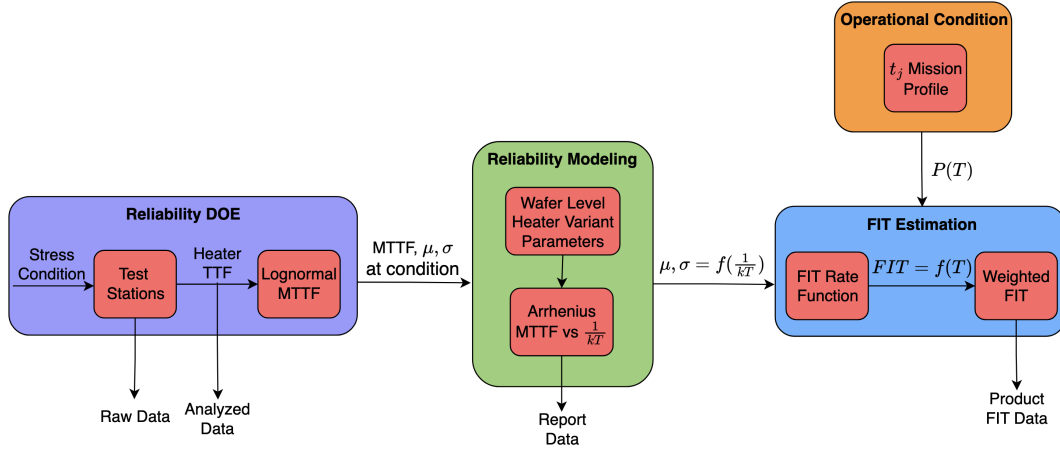


Fig. 5: Flowchart of the automated FIT analysis from test station data generation to final device FIT.

T equals the number of failures of 1 billion devices each operating for T time, and dividing by T yields the number of failures in 1 billion device-hours. Finally, we generate a weighted FIT for each heater design instantaneously using the product mission profile of junction temperature over the target lifetime, allowing for data-driven process monitoring for rapid feedback on design efficacy and volume production. Real-time data monitoring has greatly improved cross-functional data transparency and revealed location dependent trends during testing. All results are published in the internal database for easily accessible cross-design analysis.

IV. CHALLENGES IN HARDWARE DEVELOPMENT

In the pursuit of total automation integration, the key criteria for success are quality, repeatable, and traceable test data. For emerging SiPh technologies, testing and reliability are still fairly new and do not have widespread adoption of common solutions. Isolation of devices for accurate parameter characterization requires complex calibration sequences on custom stations and specially designed test chips. These custom stations are dependent on mixed control architecture and python-based orchestration integrating optical and electrical validation equipment that suffers from interface synchronization and error handling challenges. Highly intricate SiPh structures for high speed data transfer have link budgets that require high optical power input during operation that is difficult to recreate safely in the lab. Accelerated stress testing at statistically significant conditions above maximum operational power (P_{max}) is essential for reliability modeling of optical power handling, but the scalability is limited by large, expensive tunable source lasers and amplifiers that are not easily integrated into rack testing configurations.

As discussed in Section II, wafer testing hardware is extremely sensitive even when designed with fully controlled environments in the cleanroom. Prober fiber drift will impact the quality of data if not realigned between tests or within longer tests [40]. Experimental data in Fig. 6 shows the insertion loss over wavelength through the DUT without

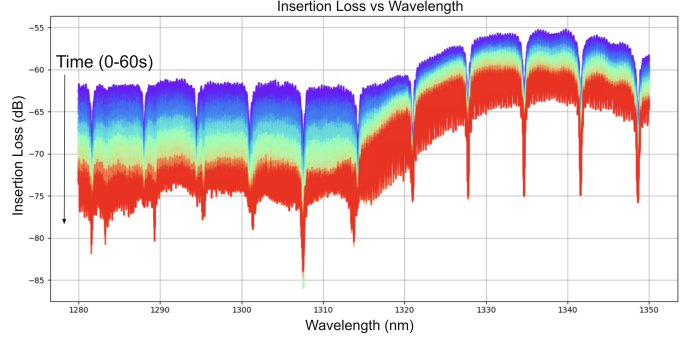


Fig. 6: Insertion loss through the DUT versus wavelength over time measured on the wafer prober at low power.

fiber realignment and fiber height control at 30 μm from the wafer. Each swept wavelength was measured from 0 to 60s (blue to red), resulting in a ~ 15 dB loss after 1 minute of data collection without realignment. Periodic dips in the data correspond to the micro-ring full spectrum resonances and are expected. Gross decrease in insertion loss after 1320 nm is also expected due to the wavelength filters of the tested coupler. Longer test times during reliability soak testing accidentally revealed a consistent, non-random periodic response of the measured optical power with 0.5 dB amplitude that did not correlate to the known fiber drift. Plotting the fast Fourier transform (FFT) of the power output at an isolated condition showed spikes every ~ 24 minutes that were consistent with oscillations in the experimental data (Fig. 7). The phenomenon seemed independent of the test sequence and was likely due to ambient conditions in the cleanroom. Temperature and humidity metrics collected in Fig. 7 (b) and (c) over 24 hours had the same peak prominence at 24-minute intervals. This indicates that part of the optical train has a temperature or humidity dependent insertion loss that is affected by the HVAC cycle as the cleanroom temperature repeatedly heats up to 70°F, triggers the AC, and cools down to the 66°F setpoint. To isolate the source of error, we can reduce the optical train

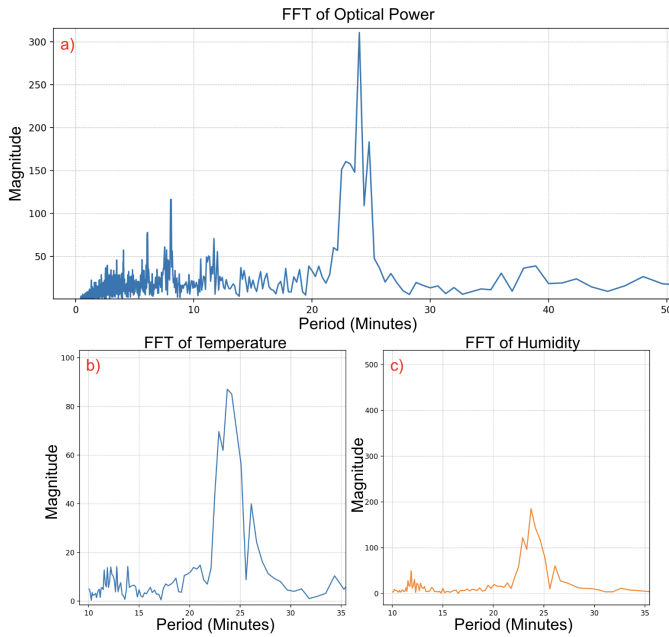


Fig. 7: FFT of measured (a) output DUT power at OPM (b) temperature of the cleanroom (c) humidity of the cleanroom.

down to a laser source and power meter with a patch cable and run the same power stability tests, then slowly add instruments back into the train one at a time.

V. SUMMARY AND NEXT STEPS

We present a path towards fully automated high-throughput silicon photonic test and reliability validation of the Ayar Labs TeraPHY optical engine using custom architectures and analysis flows with design-relevant experimental results. The wafer level optical damage setup uses a two-probe, electro-optical wafer prober and elaborate optical instrumentation for an early reliability assessment of power handling up to $P_{max} + 2$ dB on high risk PIC components. Ultra-fine prober movement capability with this test case easily supports automated nonlinear loss wafer maps. In packaged parts, in-situ monitoring of micro-ring heater current data over 1000-hour long-term degradation stress generates live NiSi electromigration heatmaps of 17 variants simultaneously. FIT analysis flows trigger immediately after stress completion to produce raw, analyzed, and report data with traceable material information. There are still many opportunities for improvement in software and hardware at low-volume applications that will stall HVM integration if not addressed. Probe drift during testing causes a 15 dB loss during the test time, requiring constant fiber realignment and increasing test time. Seemingly trivial cleanroom HVAC causes power oscillations observable only in continuous 24 hour test cases. Increasing operational power requirements for next generation CPO poses a threat to safety in the lab. Production-ready infrastructure will require continuous development and continuous integration of innovative, closed-loop solutions into existing architecture with high-yield, high-efficiency capacity.

ACKNOWLEDGEMENTS

This work was supported by Ayar Labs. The authors would like to thank the members of the engineering group for their contributions to the paper, the women's group for their support, and Jie Xue for her idea to collaborate. We also thank our OSAT partners for their contributions to testing.

REFERENCES

- [1] C. Xiang, S. M. Bowers, A. Bjorlin, R. Blum, and J. E. Bowers, "Perspective on the future of silicon photonics and electronics," *Applied Physics Letters*, vol. 118, no. 22, 2021.
- [2] I. A. Young, E. Mohammed, J. T. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. Chang, "Optical i/o technology for tera-scale computing," *IEEE Journal of solid-state circuits*, vol. 45, no. 1, pp. 235–248, 2009.
- [3] S. Y. Siew, B. Li, F. Gao, H. Y. Zheng, W. Zhang, P. Guo, S. W. Xie, A. Song, B. Dong, L. W. Luo *et al.*, "Review of silicon photonics technology and platform development," *Journal of Lightwave Technology*, vol. 39, no. 13, pp. 4374–4389, 2021.
- [4] A. Rahim, T. Spuesens, R. Baets, and W. Bogaerts, "Open-access silicon photonics: Current status and emerging initiatives," *Proceedings of the IEEE*, vol. 106, no. 12, pp. 2313–2330, 2018.
- [5] Y. Shen, X. Meng, Q. Cheng, S. Rumley, N. Abrams, A. Gazman, E. Manzhosov, M. S. Glick, and K. Bergman, "Silicon photonics for extreme scale systems," *Journal of Lightwave Technology*, vol. 37, no. 2, pp. 245–259, 2019.
- [6] A. Barkai, Y. Chetrit, O. Cohen, R. Cohen, N. Elek, E. Ginsburg, S. Litski, A. Michaeli, O. Raday, D. Rubin *et al.*, "Integrated silicon photonics for optical networks," *Journal of Optical Networking*, vol. 6, no. 1, pp. 25–47, 2007.
- [7] E. R. Fuchs, R. E. Kirchain, and S. Liu, "The future of silicon photonics: not so fast? insights from 100g ethernet lan transceivers," *Journal of Lightwave Technology*, vol. 29, no. 15, pp. 2319–2326, 2011.
- [8] C. Kopp, S. Bernabe, B. B. Bakir, J.-M. Fedeli, R. Orobtcouk, F. Schrank, H. Porte, L. Zimmermann, and T. Tekin, "Silicon photonic circuits: on-chip integration, fiber optical coupling, and packaging," *IEEE Journal of selected topics in quantum electronics*, vol. 17, no. 3, pp. 498–509, 2010.
- [9] R. Baets, P. Dumon, W. Bogaerts, G. Roelkens, D. Taillaert, B. Luysaert, G. Priem, G. Morthier, P. Bienstman, and D. Van Thourhout, "Silicon-on-insulator based nano-photonics: Why, how, what for?" in *IEEE International Conference on Group IV Photonics*, 2005. 2nd. IEEE, 2005, pp. 168–170.
- [10] M. Wade, E. Anderson, S. Ardalani, P. Bhargava, S. Buchbinder, M. L. Davenport, J. Fini, H. Lu, C. Li, R. Meade *et al.*, "Teraphy: a chiplet technology for low-power, high-bandwidth in-package optical i/o," *IEEE micro*, vol. 40, no. 2, pp. 63–71, 2020.
- [11] Z. Lu, J. Hjoja, J. Klein, X. Wang, A. Liu, J. Flueckiger, J. Pond, and L. Chrostowski, "Performance prediction for silicon photonics integrated circuits with layout-dependent correlated manufacturing variability," *Optics express*, vol. 25, no. 9, pp. 9712–9733, 2017.
- [12] N. Feilchenfeld, K. Nummy, T. Barwicz, D. Gill, E. Kiewra, R. Leidy, J. S. Orcutt, J. Rosenberg, A. Stricker, C. Whiting *et al.*, "Silicon photonics and challenges for fabrication," in *Advanced Etch Technology for Nanopatterning VI*, vol. 10149. SPIE, 2017, p. 101490D.
- [13] L. Liao, S. Fatholouloumi, K. Nguyen, H. Mahalingam, D. Hui, J. Heck, H. Frish, R. Defrees, C. Malouin, P. Seddighian *et al.*, "Silicon photonics for next-generation optical connectivity," in *2023 Optical Fiber Communications Conference and Exhibition (OFC)*. IEEE, 2023, pp. 1–3.
- [14] P. Agnihotri, P. Kalla, and S. Blair, "Silicon photonics testing: Design for testability, fault detection, and manufacturing variation analysis in photonic integrated circuits," *arXiv preprint arXiv:2606.08885*, 2026.
- [15] H. Hsia, S. Tai, C. Liu, C. Tseng, S. Lu, Y. Wu, C. Chang, J. Wu, K. Yee, C. Wu *et al.*, "Integrated optical interconnect systems (iois) for silicon photonics applications in hpc," in *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*. IEEE, 2023, pp. 612–616.
- [16] C. Douglas, C.-T. Wang, and H. Hsia, "Foundry perspectives on 2.5 d/3d integration and roadmap," in *2021 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2021, pp. 3–7.

- [17] H. Hsia, C.-H. Tsai, K.-C. Ting, F.-W. Kuo, C.-C. Lin, C.-T. Wang, S.-Y. Hou, W.-C. Chiou, and D. C. Yu, "Heterogeneous integration of a compact universal photonic engine for silicon photonics applications in hpc," in *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*. IEEE, 2021, pp. 263–268.
- [18] W. Bogaerts, M. Fiers, and P. Dumon, "Design challenges in silicon photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 4, pp. 1–8, 2013.
- [19] X. Chen, M. Mohamed, Z. Li, L. Shang, and A. R. Mickelson, "Process variation in silicon photonic devices," *Applied optics*, vol. 52, no. 31, pp. 7638–7647, 2013.
- [20] P. Agnihotri, S. K. Goel, F. Lee, and K. Chakrabarty, "Toward efficient and scalable testing of silicon photonic systems," *IEEE Design & Test*, 2026.
- [21] M. Mohamed, Z. Li, X. Chen, L. Shang, and A. R. Mickelson, "Reliability-aware design flow for silicon photonics on-chip interconnect," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 8, pp. 1763–1776, 2013.
- [22] P. De Heyn, J. De Coster, P. Verheyen, G. Lepage, M. Pantouvaki, P. Absil, W. Bogaerts, J. Van Campenhout, and D. Van Thourhout, "Fabrication-tolerant four-channel wavelength-division-multiplexing filter based on collectively tuned si microrings," *Journal of lightwave technology*, vol. 31, no. 16, pp. 3085–3092, 2013.
- [23] D. Dai, L. Yang, and S. He, "Ultrasmall thermally tunable microring resonator with a submicrometer heater on si nanowires," *Journal of Lightwave Technology*, vol. 26, no. 6, pp. 704–709, 2008.
- [24] W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing," *Optics express*, vol. 18, no. 23, pp. 23 598–23 607, 2010.
- [25] S. Hu, A. Stricker, K. McLean, C. Ma, S. G. Roy, D. Percy, J. Cartier, D. Clark, R. Van Roijen, B. Green *et al.*, "Fully automated in-line optical test system: Advanced materials & photonics," in *2018 29th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*. IEEE, 2018, pp. 399–402.
- [26] S. Arnold, "Automatic testing of photonics components: Fast, accurate, and suitable for industry," *Optik & Photonik*, vol. 11, no. 3, pp. 21–23, 2016.
- [27] J. De Coster, P. De Heyn, M. Pantouvaki, B. Snyder, H. Chen, E. J. Marinissen, P. Absil, J. Van Campenhout, and B. Bolt, "Test-station for flexible semi-automatic wafer-level silicon photonics testing," in *2016 21th IEEE European Test Symposium (ETS)*. IEEE, 2016, pp. 1–6.
- [28] R. Polster, L. Y. Dai, M. Oikonomou, Q. Cheng, S. Rumley, and K. Bergman, "Challenges and solutions for high-volume testing of silicon photonics," in *Silicon Photonics XIII*, vol. 10537. SPIE, 2018, p. 1053703.
- [29] R. Polster, L. Y. Dai, O. A. Jimenez, Q. Cheng, M. Lipson, and K. Bergman, "Wafer-scale high-density edge coupling for high throughput testing of silicon photonics," in *Optical Fiber Communication Conference*. Optica Publishing Group, 2018, pp. M3F–2.
- [30] R. W. Herrick, "Reliability testing for silicon photonics and optoelectronics," in *2024 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2024, pp. 1–10.
- [31] JEDEC, "Jesd264: Silicon photonics qualification and reliability requirements," 2026.
- [32] J. De Coster, E. J. Marinissen, J. Van Campenhout, B. Bolt, and D. Rishavy, "Developing silicon photonics technologies with a wafer-level test station," *imec Magazine*, 2018.
- [33] W.-Y. Hsu, "Silicon photonic wafer testing system and testing method thereof," U.S. Patent Application Publication US 2026/0210800 A1, Jul. 23, 2026.
- [34] I. Shake, H. Takara, and S. Kawanishi, "Simple measurement of eye diagram and ber using high-speed asynchronous sampling," *Journal of lightwave technology*, vol. 22, no. 5, p. 1296, 2004.
- [35] M. Tan, J. Xu, S. Liu, J. Feng, H. Zhang, C. Yao, S. Chen, H. Guo, G. Han, Z. Wen *et al.*, "Co-packaged optics (cpo): status, challenges, and solutions," *Frontiers of optoelectronics*, vol. 16, no. 1, p. 1, 2023.
- [36] N. Mehta, S. Lin, B. Yin, S. Moazeni, and V. Stojanović, "A laser-forwarded coherent transceiver in 45-nm soi cmos using monolithic microring resonators," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1096–1107, 2020.
- [37] J. C. Sturm and C. M. Reaves, "Silicon temperature measurement by infrared absorption. fundamental processes and doping effects," *IEEE Transactions on electron devices*, vol. 39, no. 1, pp. 81–88, 1992.
- [38] Y.-L. Cheng, M.-K. Shiao, W.-Y. Chung, and Y.-L. Wang, "Competition of electromigration reliability in copper and nickel-silicide," *Journal of The Electrochemical Society*, vol. 158, no. 2, pp. H174–H177, 2011.
- [39] J. Lienig and M. Thiele, "Fundamentals of electromigration," in *Fundamentals of electromigration-aware integrated circuit design*. Springer, 2018, pp. 13–60.
- [40] M. J. Bitting, "Optical switching for automated test systems," in *Proceedings, IEEE AUTOTESTCON*. IEEE, 2002, pp. 140–151.