

Split-Gate Inter-Poly Architecture for Electrical Gate Leakage and Mechanical Wafer Warpage Optimization in Trench FP-MOSFETs

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Abstract — Mechanical wafer warpage is a critical challenge in advanced Trench Field-Plate MOSFETs (FP-MOSFETs), becoming more severe with deeper trenches and higher trench densities. In wafer fabrication plants, high warpage causes severe mechanical robot handling failures and lithography depth-of-focus degradation. While lower temperature processing (below 1000 °C) mitigates warpage, it fails to fully anneal out split-gate inter-poly oxide charges, thereby degrading device electrical performance. To resolve this stress-performance trade-off, this paper proposes a novel split-gate architecture featuring a robust inter-poly structure that physically and electrically isolates the polysilicon layers. This architecture effectively suppresses leakage paths while fully preserving the warpage reduction achieved through thermal optimization. Experimental results demonstrate a practical solution that balances mechanical stress mitigation with high inter-poly oxide integrity.

Keywords—SGT (Split-Gate Trench) Power MOSFET, interpoly leakage current, wafer warpage.

I. INTRODUCTION

In the rapidly evolving power electronics landscape, there is a growing demand for switching devices that deliver high efficiency, reliability, and compactness. Field Plate Power MOSFETs (FP-MOSFETs) have become a key technology in low-voltage applications such as inverters, motor control systems, and switch-mode power supplies (SMPS). These devices are specifically designed to meet the stringent performance and robustness requirements of modern power systems.^[1,12] By optimizing capacitances and electric field distribution, FP-MOSFETs effectively reduce switching losses and electrical stress, enabling faster switching speeds without sacrificing efficiency^[7-9].

Wafer warpage is a key challenge in silicon wafer manufacturing, caused by CTE mismatch between process materials and the substrate^[3]. The resulting thermal stress leads to compressive or tensile deformation, which can disrupt alignment, handling, and patterning, increase scratch defects, and reduce yield^[5]. Controlling warpage is therefore essential for stable processing and reliable device quality.

In this study, critical warpage-contributing process steps were first identified to support targeted optimization. Based on this analysis, a novel inter-poly structure was developed and successfully fabricated. The new design not only reduced wafer warpage but also improved the electrical performance

of the FP-MOSFET, demonstrating a combined benefit for manufacturability and device characteristics.

II. CHALLENGES OF WARPAGE IN DEVICE FABRICATION

The wafer warpage changes during the fabrication in silicon wafers on N-type, 200 mm diameter was collected as shown in Fig. 1.

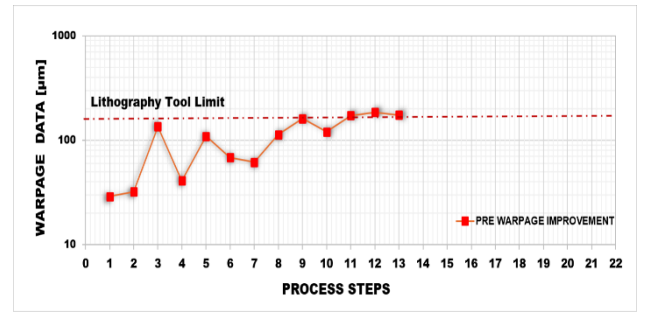


Fig.1. Warpage changes of Silicon wafer during the process flow. Step 1-2: Trench fabrication; Step 3-6: Trench Field-Plate ; Step 7-12: Gate Poly-Silicon process with high thermal budget process involved contributing significantly to wafer warpage accumulation ; Step 13-15: Channel formation; Step 16-18: Contact and Metallization; Step 19-20: Wafer Passivation; Step 21-22: Back metallization

After process #10, the wafer underwent irreversible warpage beyond the lithography tool specification, indicating that the accumulated thermal/mechanical stress exceeded the wafer's elastic recovery limit. And so, the wafer could not be properly flattened on the chuck, causing focus instability, overlay drift, and poor clamping during exposure. This led to handling and chucking failures, approximately 25% scrap during inline processing, and reduced overall manufacturability.

III. WARPAGE CONTROL TECHNIQUES

To reduce the warpage, various design of experiments [DOEs] was conducted to balance the stress on both front and back sides of the wafer.

Table 1. DOEs Summary on Warpage control techniques

#	DOE	OUTCOME
A	Trench Design	Positive, but no impact on subsequent inline warpage
B	Pre-bowing Wafer Compensation strategy	Negative
C	Effects of Film temperature	Positive

A. Trench Design

The initial unidirectional trench design created asymmetric stress and stiffness, increasing wafer warpage to $\sim 130\ \mu\text{m}$ by process step #3. Introducing transversal trench patterns improved stress redistribution, reduced asymmetric bending, and lowered warpage to $\sim 40\ \mu\text{m}$, corresponding to a $\sim 68\%$ reduction. However, this approach was insignificant to downstream inline processes, although with this change full process wafer warpage was substantially reduced, as shown in Fig. 2.

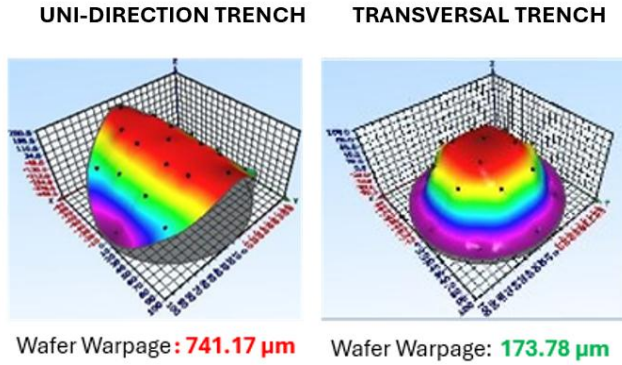


Fig. 2. Total warpage measured after wafer finishing process Uni-direction vs Transversal Trench

B. Pre-Bowing wafer compensation strategy

As shown in Fig. 2, the wafer has warped to a dome-shaped profile over the fabrication processes due to frontside-backside stress imbalance. Pre-bowing compensation using both tensile- and compressive-stress films was investigated to balance coefficient of thermal expansion (CTE)-driven stress mismatch within the wafer stack. However, the experiment showed no significant warpage improvement, indicating that film deposition and removal were insufficient to compensate for the dominant intrinsic stress and thermal mismatch effects.

C. Effects of film temperature

Process step 7-12, involving gate-polysilicon formation at high temperature, contributes significantly to silicon plastic deformation, making CTE matching largely ineffective for warpage control. During high temperature process, wafers are exposed to rapid temperature ramp-up and prolonged exposure to heat deforms the wafer irreversibly. Experiments with gradual temperature increase showed no measurable improvement.

A more effective approach was achieved by reducing the oxidation temperature while maintaining oxide quality, which reduced thermal budget-induced deformation and lowered wafer warpage to about 25%. However, subsequent high-temperature annealing reintroduced severe thermal stress, increasing warpage to $>170\ \mu\text{m}$ with no further recovery. The improvements achieved in earlier processes are effectively negated when the wafer undergoes these

high-temperature cycles, resulting in increased warpage. Following a thorough evaluation of both design and process factors, Process #13 was intentionally omitted to suppress inline warpage accumulation.

With these changes, wafer warpage improved by approximately 30%, as shown in Fig. 3(a). The final wafer warpage after full fabrication was reduced to around $30\ \mu\text{m}$.

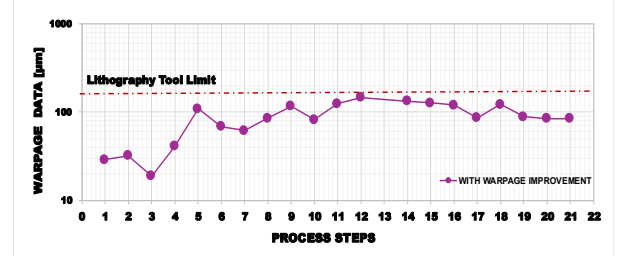


Fig. 3. Warpage changes of Silicon wafer With Warpage Improvement Techniques

IV. BALANCING WARPAGE AND ELECTRICAL PERFORMANCE

While wafer warpage improved, Fig. 4(a) shows a significant degradation in gate leakage, reaching $9\ \mu\text{A}$ at $20\ \text{V}$ versus the $200\ \text{nA}$ target. This indicates that the warpage-reduction process changes compromised electrical integrity and device reliability. In the trench FP MOSFET structure, the thin top enclosure region between the gate polysilicon and gate oxide is vulnerable to gate shorts. Omitting Process #12 prevented full dissipation of residual charges trapped within the inter-polysilicon layer. This leads to increased gate leakage caused by a combination of factors: high electric field concentration at the field plate edges, defects in the gate oxide, process-induced damage, and material imperfections at the gate oxide-polysilicon interface.^[9-10] This insight prompted to consider redesigning the device structure without reverting to pre-warpage control process steps. To address these challenges and enhance device performance, a novel split-gate inter-polysilicon structure has been developed, aiming to alleviate field concentration.

This new architectural design requires minimal modifications to the existing process flow. The primary changes occur in the gate formation module, where a polysilicon mask step is intentionally skipped. As a result, the polysilicon is not planarized to the wafer surface and remains protruded. The subsequent recess etch selectively impacts the oxide layer without affecting the polysilicon. Following this, the polysilicon undergoes oxidation with a low-temperature gate oxide, after which it is covered by the polysilicon deposited in the subsequent process step.

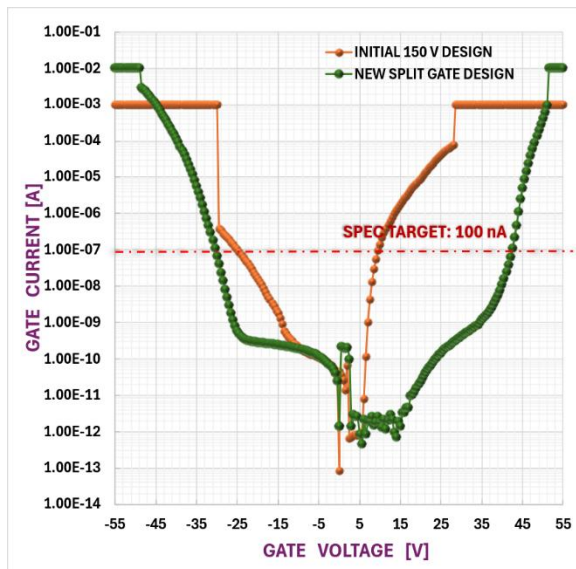


Fig. 4. (a) Electrical Characteristics of Gate Current vs Gate Voltage after Warpage control techniques implemented (b) Electrical Characteristics of Gate Current vs Gate Voltage of the Noval Architecture design

The split gate design, as shown in Fig.5 (b), offers several advantages in reducing gate leakage. By physically dividing the gate polysilicon, the effective surface area of the gate polysilicon–inter-poly oxide interface is significantly reduced. This reduction lowers the probability of leakage paths forming along the oxide interface, especially in the critical top enclosure areas that were previously prone to shorts. Additionally, splitting the gate mitigates high electric field concentrations by distributing the potential more evenly across the gate structure, thereby reducing localized stress on the gate oxide. This architectural change also minimizes defect accumulation and process-induced damage in vulnerable regions, improving overall device reliability.

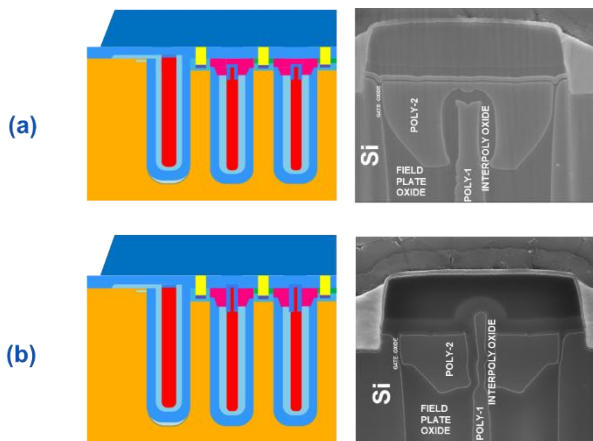


Fig. 5 (a) Cross Schematic and XSEM of the initial FP-MOSFET architecture (b) Cross Schematic and XSEM of the new architecture

Data in Fig. 4(b) show that the split-gate design effectively suppresses gate leakage, reducing the current to below 1 nA at 20 V, well within the <200 nA target specification. This improvement indicates strong suppression

of parasitic conduction paths associated with high electric-field regions and defects at the gate oxide–polysilicon interface. As a result, the split-gate structure reduces power loss and enhances device reliability and longevity, while requiring only minimal changes to the existing fabrication process.

CONCLUSION

This study addressed the critical challenge of wafer warpage in advanced Field-Plate MOSFET (FP-MOSFET) technology, where device scaling and increased trench density intensify mechanical stress. Through detailed warpage analysis and targeted process adaptations—such as lowering the gate oxidation temperature and omitting the polysilicon anneal step—inline wafer warpage was successfully reduced from 184 μm to 147 μm .

However, these mechanical improvements came with significant electrical reliability concerns, particularly increased gate leakage caused by weakened interfaces between gate polysilicon layers. To resolve this trade-off, a novel split-gate architecture was developed. By modifying the process flow—specifically skipping the polysilicon recess and implementing a low-temperature process—the polysilicon-1 and polysilicon-2 terminals are physically and electrically isolated by a robust inter-poly oxide layer. This innovation effectively eliminates inter-poly leakage paths without reintroducing excessive thermal stress, as the polysilicon anneal remains intentionally omitted to preserve warpage improvements.

Overall, this work underscores the delicate balance between mechanical and electrical optimization in advanced device fabrication. The introduced split-gate process flow provides a promising solution to simultaneously achieve reduced wafer warpage and enhanced device integrity, paving the way for reliable scaling of FP-MOSFET technology in future voltage classes.

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